NB11.6 Block Diagram

LPDDR3 4/8GB

LPDDR3 MD 1866/1600MHz X32 2PCS — 1866MT/S_Channel A — DDR CHA 2.5"

LPDDR3 MD 1866/1600MHz X 32 2PCS — 1866MT/S_Channel B — DDR CHB

SATA — SATA 6.5~7.5"

SATA3.0 — NGFF M.2 2280 SSD

WLAN BT

ANTENNA — NGFF M.2 2230 WLAN / BT Combo — PCIE(GEN1) — USB_BT

24MHz

PCIE*4

Micro SD Card Conn (SD3.0) — SD Card Reader RTS5227S Package : QFN32 Size : 4 X 4 (mm) — PCIE(GEN1)

32.768KHz

PCIE — PCIE 8"

LPC — LPC 10"

Touch PAD /Keyboard CONN — Embedded Controller IT8987VG Package : VFBGA Size : 7 X 7 (mm)

SPI — SPI 6.5"

SPI ROM

Share ROM

15" I2C

Kabylake Y Processor

Processor : Daul Core
Power : 4.0 (Watt)
Package : BGA1515
Size : 20*16.5 (mm)

eDP 6" — eDP — 11.6“FHD (1920x1080) w/o Touch

DDI 3" — HDMI — HDMI CONN

USB3.0 9"

USB3.0 — USB 3.0 A Type Conn — USB 3.0 A Type Conn

USB Charger TPS2544

USB2.0 12" — USB2.0 — USB_BT

HDA 14" — HDA — Audio CODEC ALC 286S — DMIC

External HP/Mic — Combo Jack

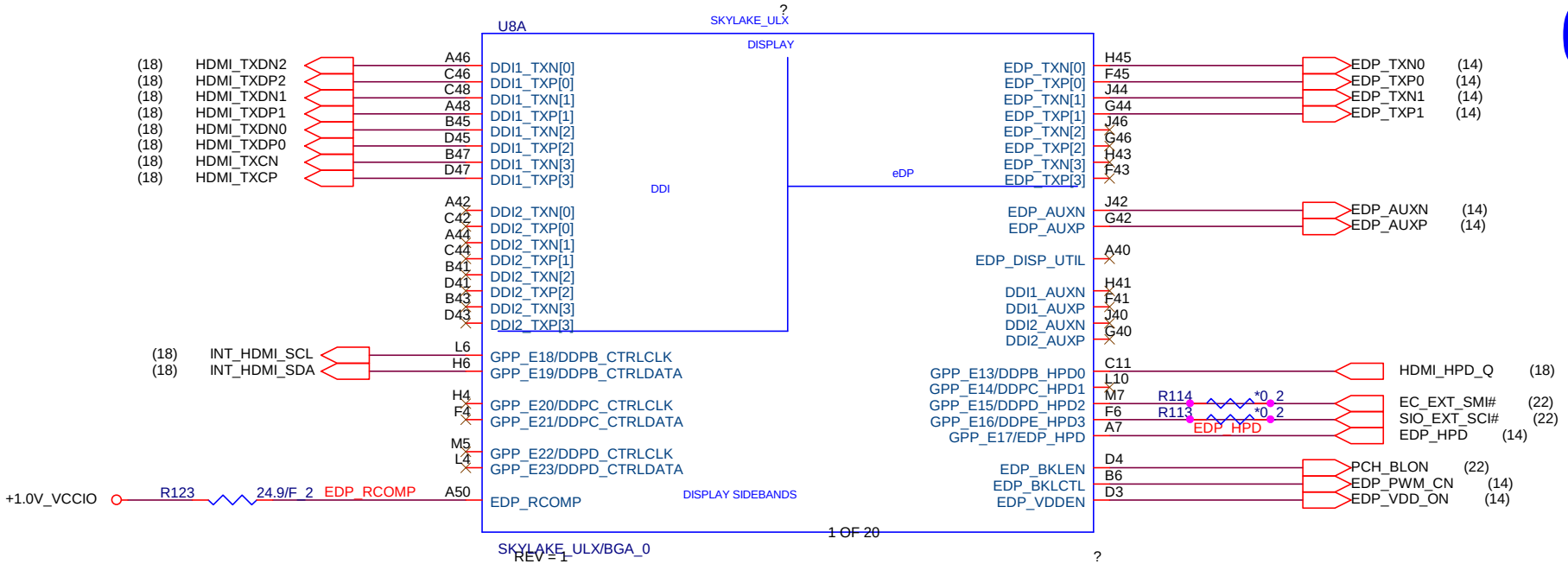
L/R — 1W Speaker x 2

FRONT Camera 0.9M (720p) — Digital MIC — Digital MIC

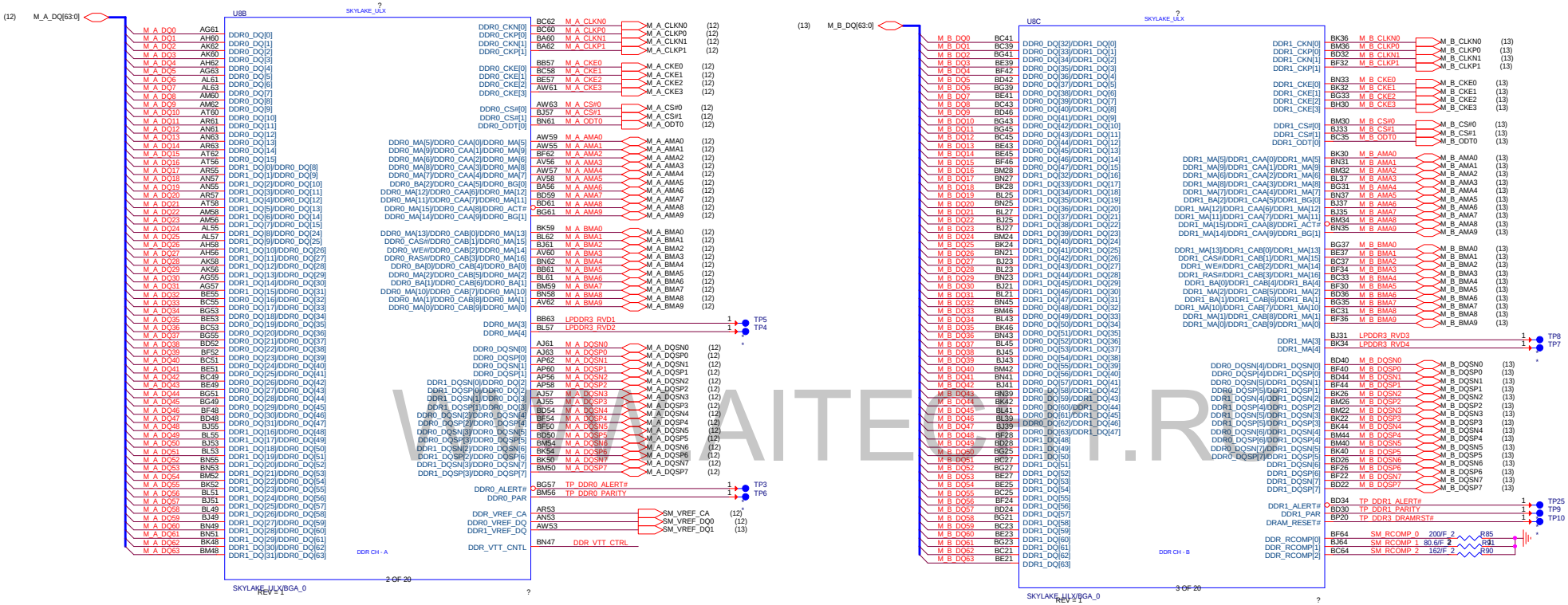
Quanta Computer Inc.
PROJECT : NN5

Size	Document Number	Rev
	Block Diagram	1A

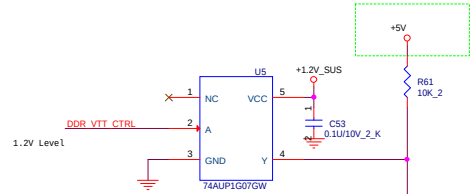
Date: Thursday, August 25, 2016 Sheet 1 of 35



Quanta Computer Inc.		
PROJECT : NN5		
Size	Document Number: SKL-Y CPU (DDI/EDP)	Rev: 1A
Date: Thursday, August 25, 2016	Sheet 2 of 35	



DDR3L SODIMM ODT GENERATION



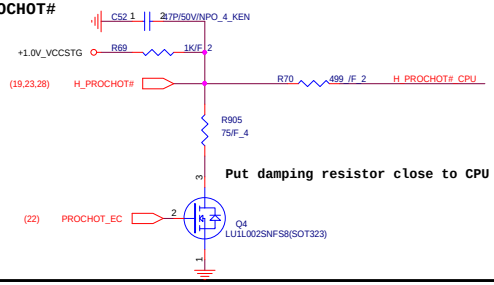
Double check DDR3L PWR

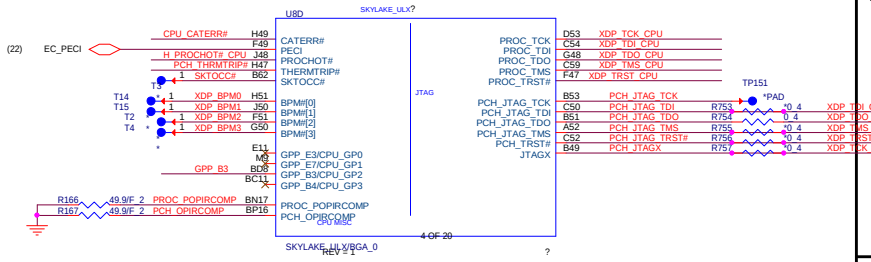
A	Y
L	L
H	Z

H = HIGH voltage level;
L = LOW voltage level;
Z = high-impedance OFF state.

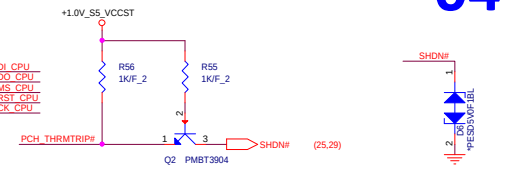
Quanta Computer Inc.		
PROJECT : NN5		
Size	Document Number	Rev 1A
	SKL-Y CPU (Memory)	
Date: Thursday, August 25, 2016	Sheet 3 of 35	

PROCHOT#



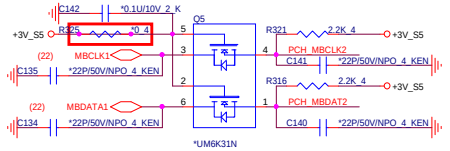


THRMTRIP

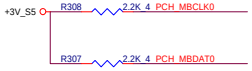


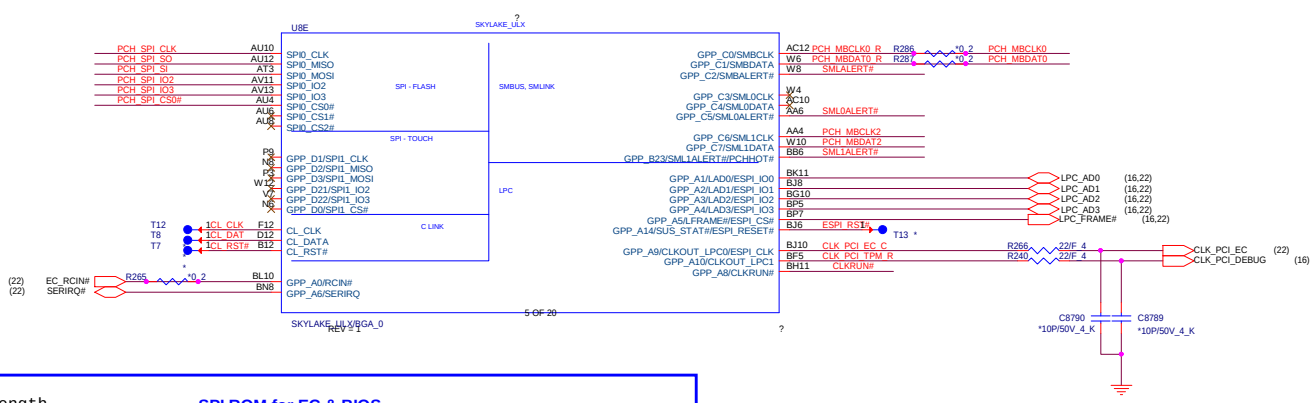
SMB TO EC

R325 non staff for cost



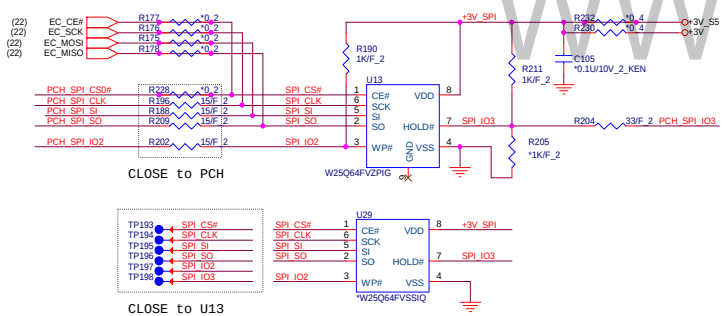
SMB

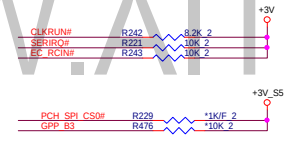


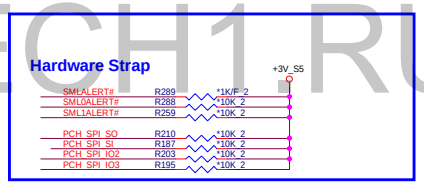


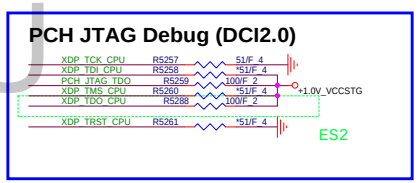
Trace Length
EC Side 6.5 inch
PCH Side 8 inch

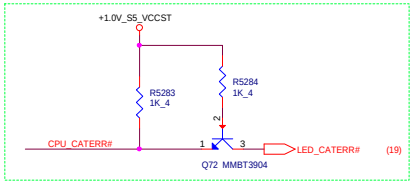
SPI ROM for EC & BIOS











Quanta Computer Inc.
PROJECT : NN5
Size
Document Number
SKL-Y CPU (MISC/JTAG/SMB)
Rev 1A
Date: Thursday, August 25, 2016
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	GPP_B22(Boot BIOS)
PU	LPC
PD	SPI (Default IPD)

U8F — SKYLAKE_ULX — LPSS / ISH

GPP_B15/GSPI0_CS# BC3
GPP_B16/GSPI0_CLK AW10
GPP_B17/GSPI0_MISO AW9
GPP_B18/GSPI0_MOSI BB4
(11) NO_REBOOT — NO_REBOOT
GPP_B19/GSPI1_CS# BB2
GPP_B20/GSPI1_CLK AW12
GPP_B21/GSPI1_MISO AW4
GPP_B22/GSPI1_MOSI AW8
+3V_S5 — R297 *1K/F_2 — GPP_B22
GPP_C8/UART0_RXD AC8
GPP_C9/UART0_TXD AA8
GPP_C10/UART0_RTS# AA10
GPP_C11/UART0_CTS# AA12
TP182 *PAD UART2_TXD — AD5
TP183 *PAD UART2_RXD — AD7
TP206 *PAD — AD3
TP207 *PAD — AD9
GPP_C20/UART2_RXD
GPP_C21/UART2_TXD
GPP_C22/UART2_RTS#
GPP_C23/UART2_CTS#
GPP_C16/I2C0_SDA AD11
GPP_C17/I2C0_SCL AB3
TP57 1 — AB9
TP56 1 — AB11
GPP_C18/I2C1_SDA
GPP_C19/I2C1_SCL
GPP_F4/I2C2_SDA AP3
GPP_F5/I2C2_SCL AP7
GPP_F6/I2C3_SDA AP5
GPP_F7/I2C3_SCL AT7
GPP_F8/I2C4_SDA AN4
GPP_F9/I2C4_SCL AN6

GPP_C is 3.3V
GPP_F is 1.8V

GPP_D9/ISH_SPI_CS# P11
GPP_D10/ISH_SPI_CLK T7
GPP_D11/ISH_SPI_MISO T5
GPP_D12/ISH_SPI_MOSI T11
GPP_D5/ISH_I2C0_SDA P7
GPP_D6/ISH_I2C0_SCL P5
GPP_D7/ISH_I2C1_SDA T9
GPP_D8/ISH_I2C1_SCL T3
GPP_F10/I2C5_SDA/ISH_I2C2_SDA AM7
GPP_F11/I2C5_SCL/ISH_I2C2_SCL AT9
GPP_D13/ISH_UART0_RXD/SML0BDATA U10
GPP_D14/ISH_UART0_TXD/SML0BCLK U4
GPP_D15/ISH_UART0_RTS# U6
GPP_D16/ISH_UART0_CTS#/SML0BALERT# V9
GPP_C12/UART1_RXD/ISH_UART1_RXD AC6
GPP_C13/UART1_TXD/ISH_UART1_TXD AC4
GPP_C14/UART1_RTS#/ISH_UART1_RTS# AB7
GPP_C15/UART1_CTS#/ISH_UART1_CTS# AB5
GPP_A18/ISH_GP0 BF11
GPP_A19/ISH_GP1 BD2
GPP_A20/ISH_GP2 BJ1
GPP_A21/ISH_GP3 BL3
GPP_A22/ISH_GP4 BJ3
GPP_A23/ISH_GP5 BD4 — ISH_GPIO5 — 1 — TP28
GPP_A12/BM_BUSY#/ISH_GP6 BJ4 — ISH_GPIO6 — 1 — TP32

6 OF 20
SKYLAKE_ULX/BGA_0
REV = 1

+3V
UART2_TXD — R292 — 49.9K/F_2
UART2_RXD — R293 — 49.9K/F_2

CLOSE to PCH

U8G — SKYLAKE_ULX — AUDIO / SDIO/SDXC

(17) HDA_SYNC — R245 33/F_2 HDA_SYNC_R — BJ19 HDA_SYNC/I2S0_SFRM
(17) HDA_BITCLK — R244 33/F_2 HDA_BITCLK_R — BK18 HDA_BLK/I2S0_SCLK
(17) HDA_SDOUT — R428 33/F_2 HDA_SDOUT_R — BK16 HDA_SDO/I2S0_TXD
(17) HDA_SDIN0 — BL15 HDA_SDI0/I2S0_RXD
(17,22) HDA_RST# — R269 33/F_2 HDA_RST#_R — BL17 HDA_SDI1/I2S1_RXD
BL19 HDA_RST#/I2S1_SCLK
V5 GPD_D23/I2S_MCLK
BL12 I2S1_SFRM
BK14 I2S1_TXD
C8788 *10P/50V_4_K

AT13 GPP_F1/I2S2_SFRM
AT11 GPP_F0/I2S2_SCLK
AP11 GPP_F2/I2S2_TXD
AT5 GPP_F3/I2S2_RXD
V3 GPP_D19/DMIC_CLK0
V11 GPP_D20/DMIC_DATA0
U12 GPP_D17/DMIC_CLK1
U8 GPP_D18/DMIC_DATA1
(11) ACZ_SPK — ACZ_SPK — AV3 GPP_B14/SPKR

Strapping_GPP_B14

GPP_G0/SD_CMD AH9 — BOARD_ID0
GPP_G1/SD_DATA0 AH11 — BOARD_ID1
GPP_G2/SD_DATA1 AG12 — BOARD_ID2
GPP_G3/SD_DATA2 AF9 — BOARD_ID3
GPP_G4/SD_DATA3 AF11 — BOARD_ID4
GPP_G5/SD_CD# AG8
GPP_G6/SD_CLK AG10
GPP_G7/SD_WP AE12
GPP_A17/SD_PWR_EN#/ISH_GP7 BL4
GPP_A16/SD_1P8_SEL BN4
SD_RCOMP BF1 — SD_RCOMP 200/F_2 — R216
GPP_F23 AJ8

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SKYLAKE_ULX/BGA_0
REV = 1

+3V
R427 10K_2 BOARD_ID0 — R439 *10K_2
R426 10K_2 BOARD_ID1 — R438 *10K_2
R425 10K_2 BOARD_ID2 — R437 *10K_2
R424 10K_2 BOARD_ID3 — R436 *10K_2
R423 10K_2 BOARD_ID4 — R435 *10K_2

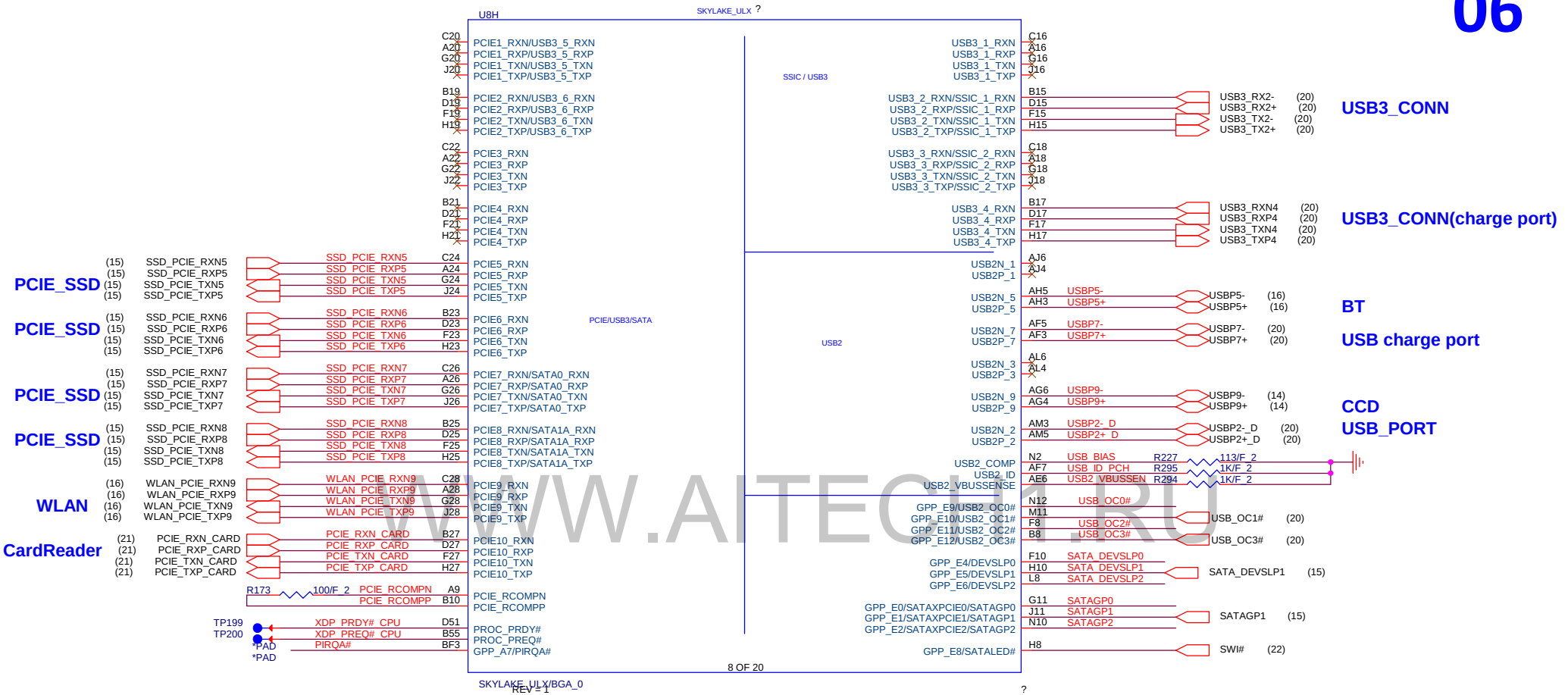
Model				BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
Samsung 4G K4E8E324EB-EGCF				0	0	0	0	0
Samsung 8G K4E6E304EB-EGCF				0	0	0	0	1
Hynix 4G H9CCNNN8GTALAR-NUD				0	0	0	1	0
Hynix 8G H9CCNNNBJTALAR-NUD				0	0	0	1	1
				0	0	1	0	0

Security Flash Descriptors

+3V_S5 — R429 *1K/F_2 — HDA_SDOUT_R — HDA_SDOUT_R (22)

Quanta Computer Inc.
PROJECT : NN5

Size	Document Number	Rev
	SKL-Y CPU (LPSS/HDA)	1A
Date: Thursday, August 25, 2016	Sheet 5 of 35	



Quanta Computer Inc.		
PROJECT : NN5		
Size	Document Number	Rev
	SKL-Y CPU (PCIE/USB3)	1A
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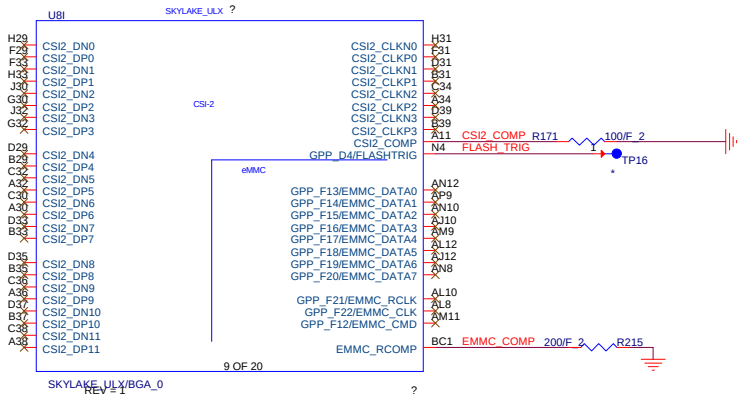
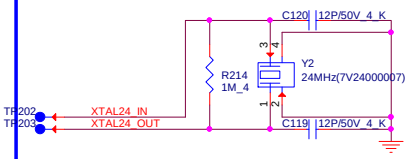
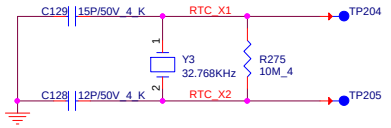
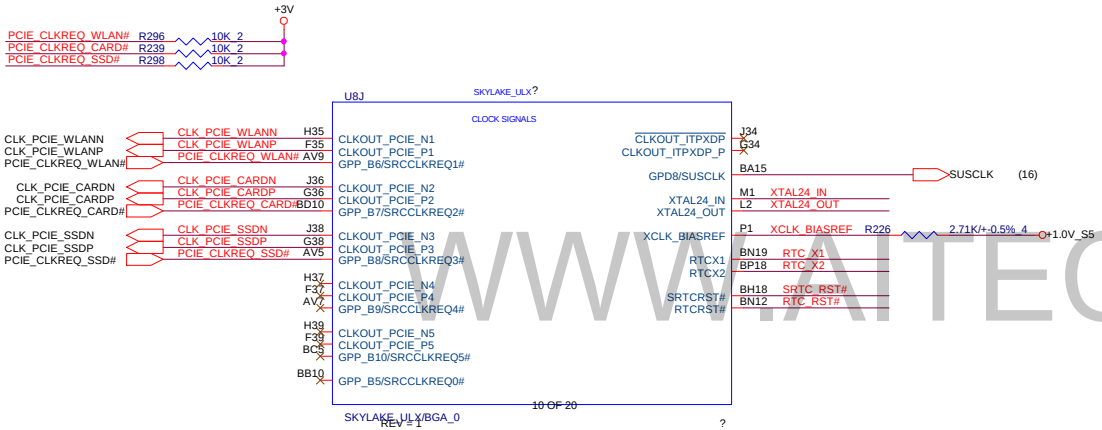


PCH Crystal (CLG)



RTC Crystal (CLG)



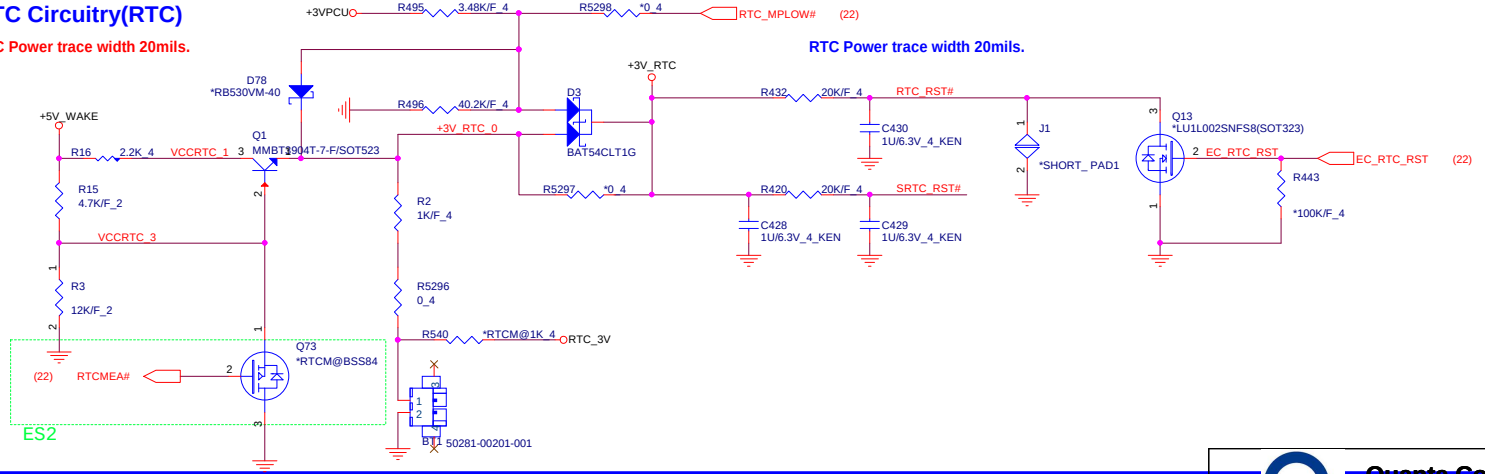


ESD request

RTC Circuitry(RTC)

RTC Power trace width 20mils.

RTC Power trace width 20mils.



Quanta Computer Inc.

PROJECT : NN5

Size	Document Number	Rev
	SKL-Y CPU (CSI2/RTC/CLK)	1A

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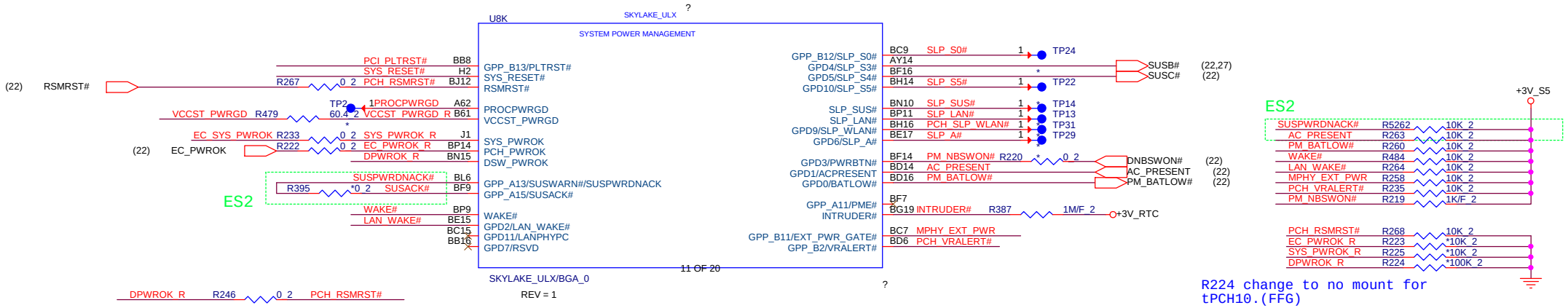
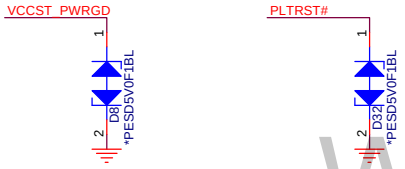
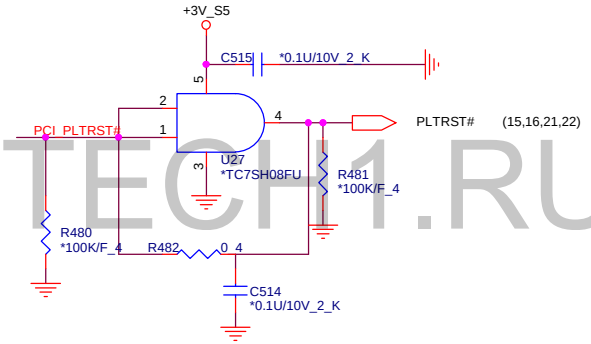
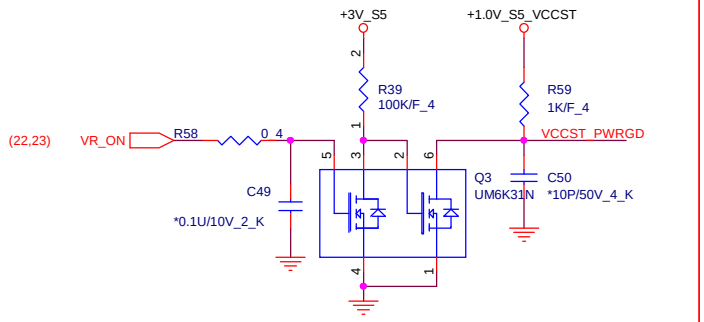


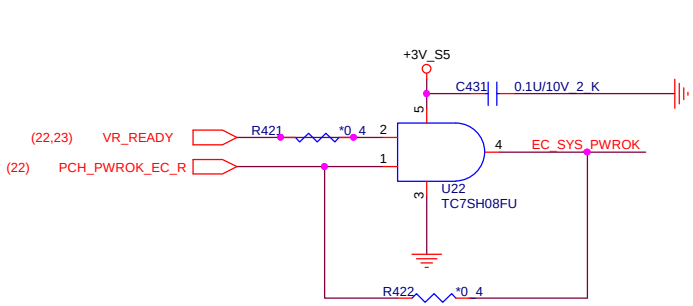




PM_BATLOW# Status

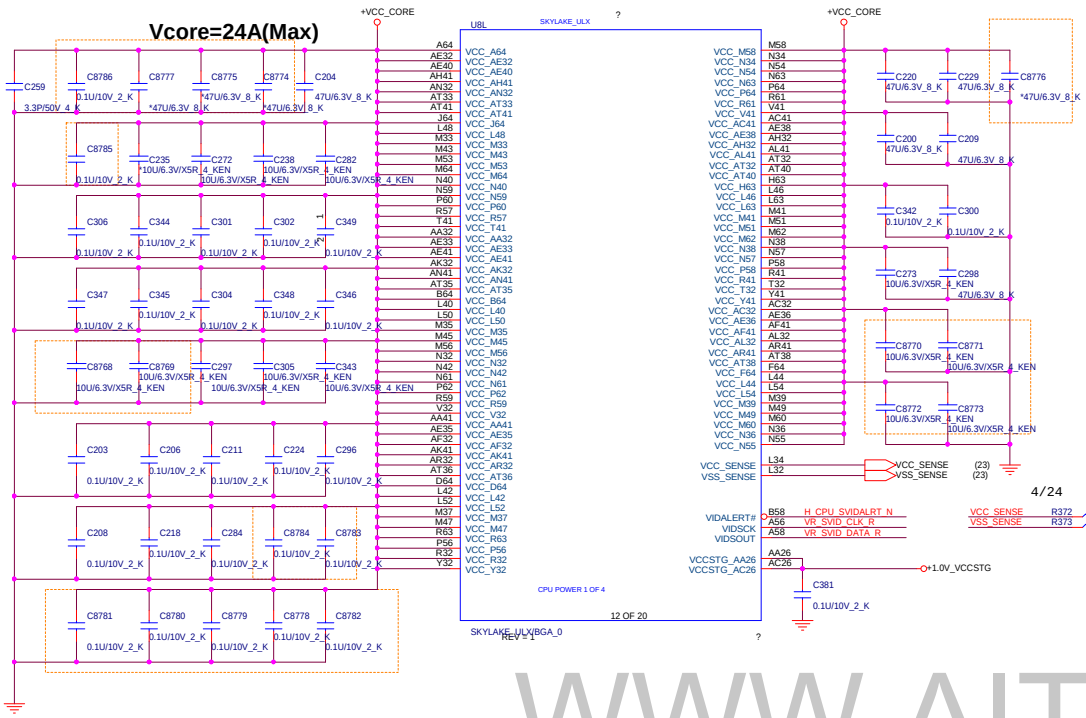
Battery Status	Low Battery		Normal	
AC Adaptor	Not plugged	Plugged	Not plugged	Plugged
BATLOW#	Low (Assert)	High (De-assert)	High (De-assert)	High (De-assert)

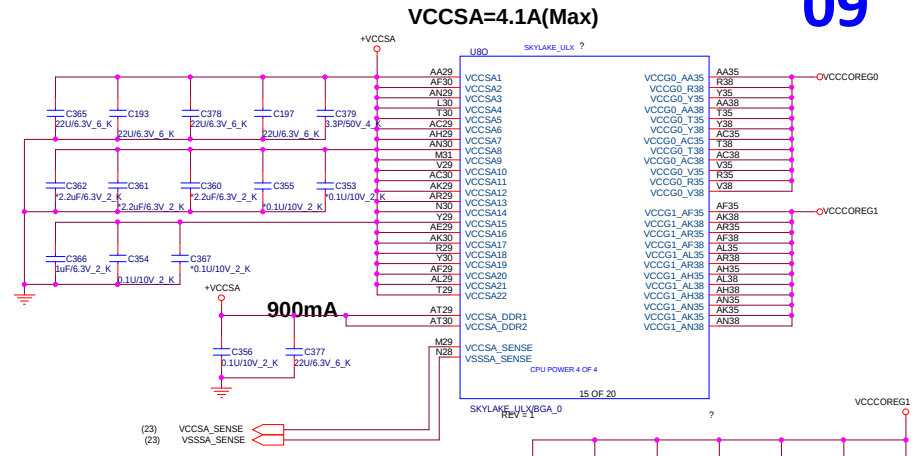


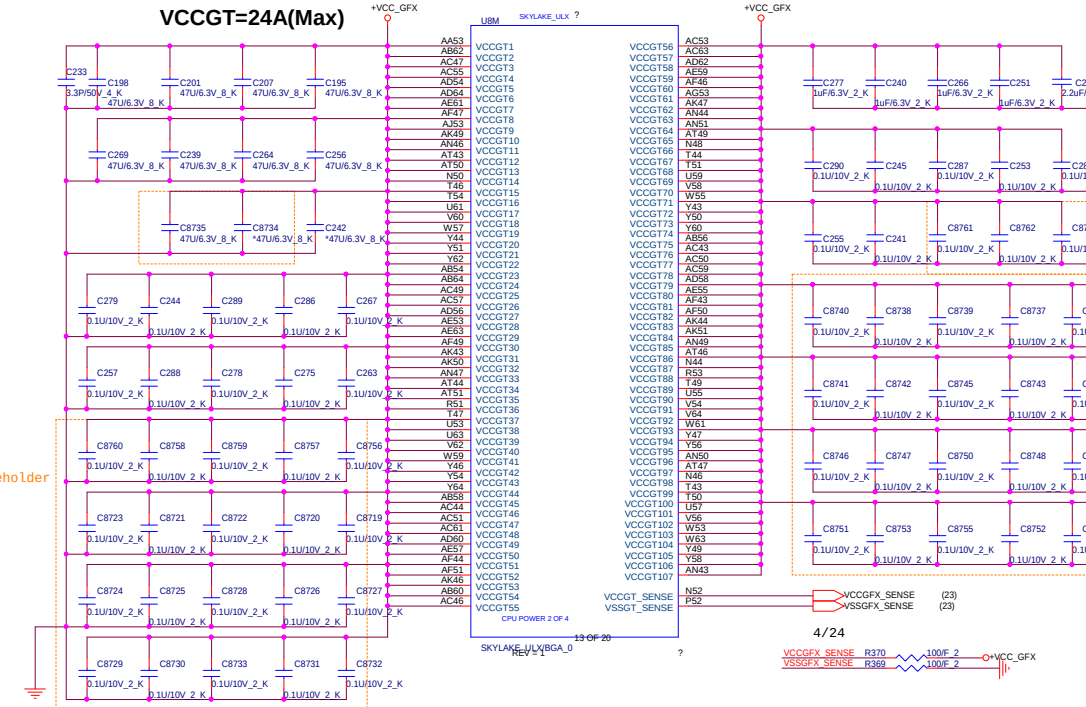


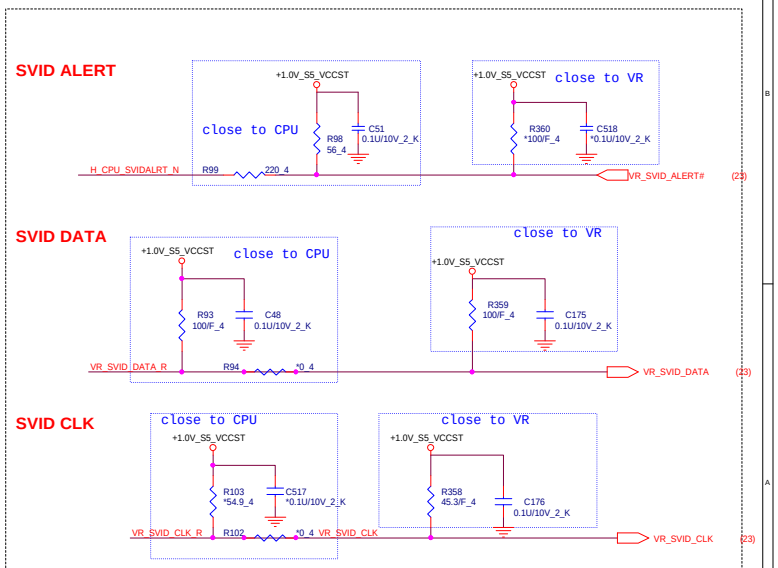
Quanta Computer Inc.
PROJECT : NN5

Size	Document Number	Rev
	SKL-Y CPU (PWR MANAGE)	1A
Date: Thursday, August 25, 2016	Sheet 8 of 35	

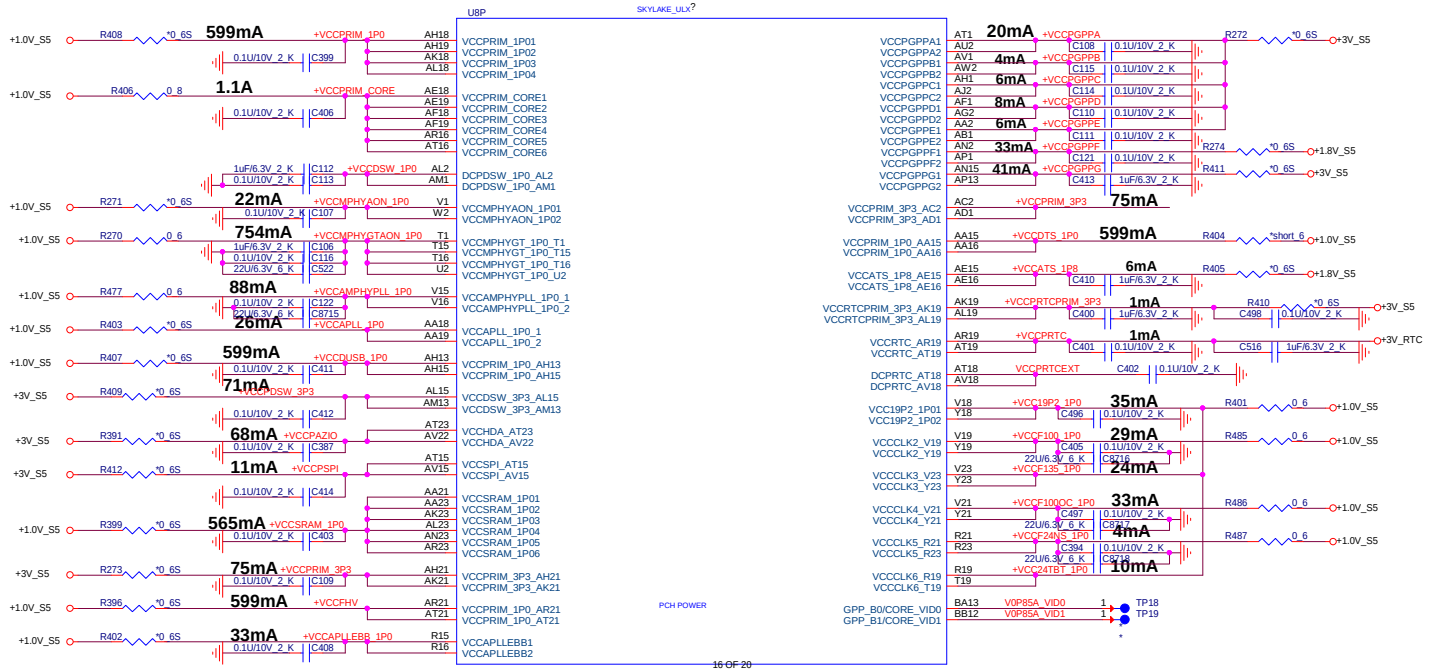


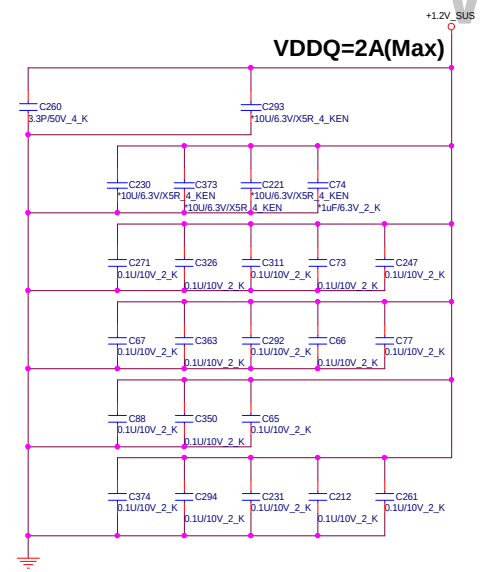


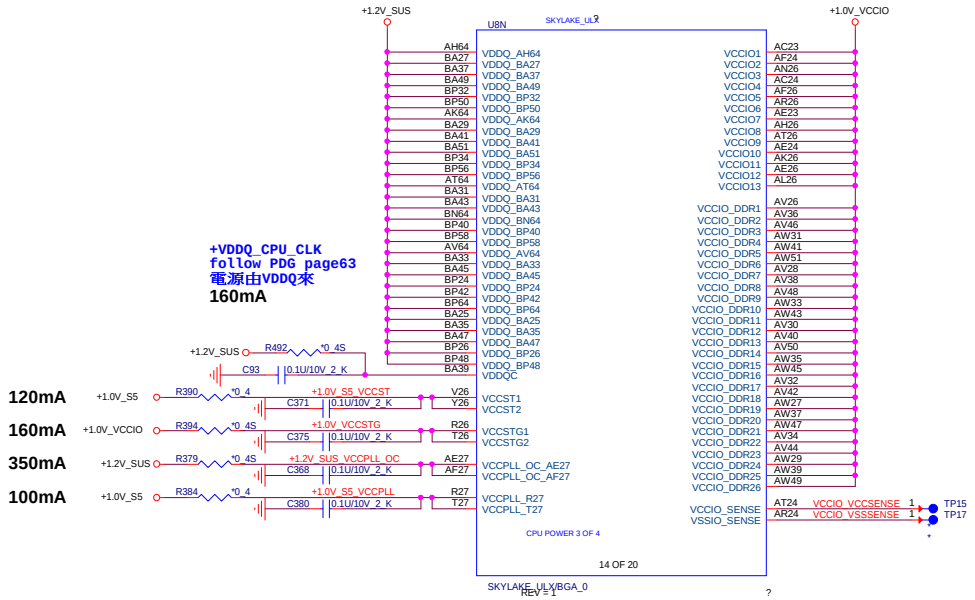


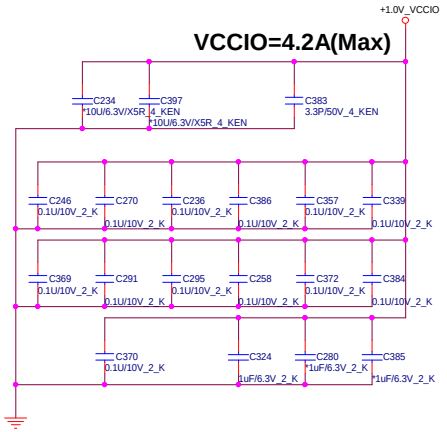


Quanta Computer Inc.		
PROJECT : NN5		
Size	Document Number	Rev
	SKL-Y CPU (PWR1)	1A
Date: Thursday, August 25, 2016	Sheet 9 of 35	

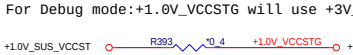




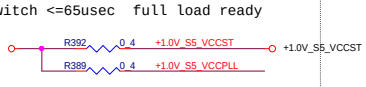




For Debug mode:+1.0V_VCCSTG will use +3V_S5 power rail



For Load switch <=65usec full load ready

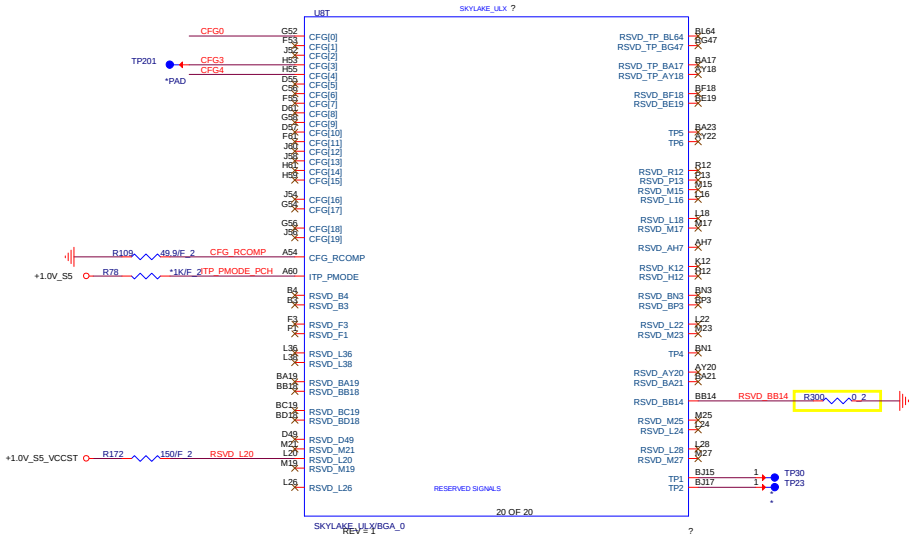


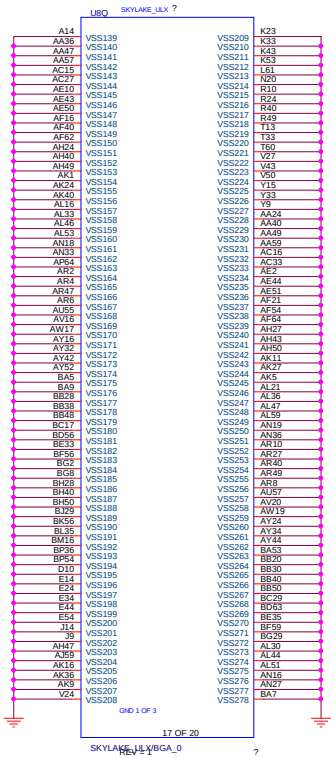
Quanta Computer Inc.

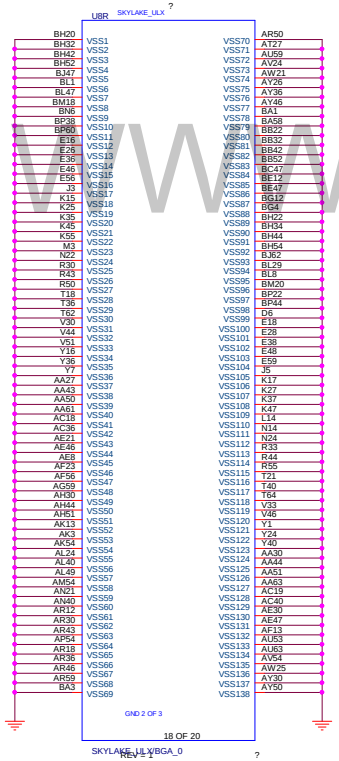
PROJECT : NN5

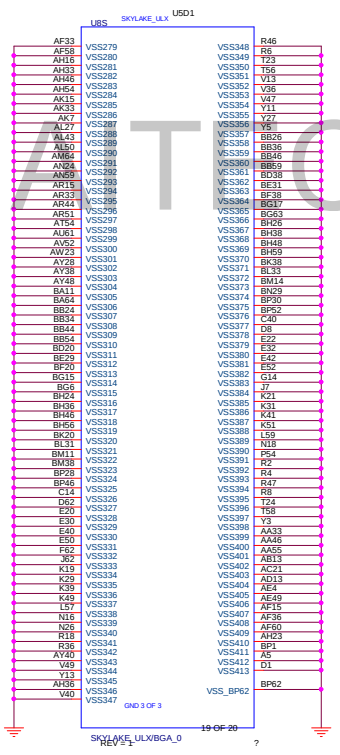
Size	Document Number	Rev
	SKL-Y CPU (PWR2)	1A

Date: Thursday, August 25, 2016 Sheet 10 of 35









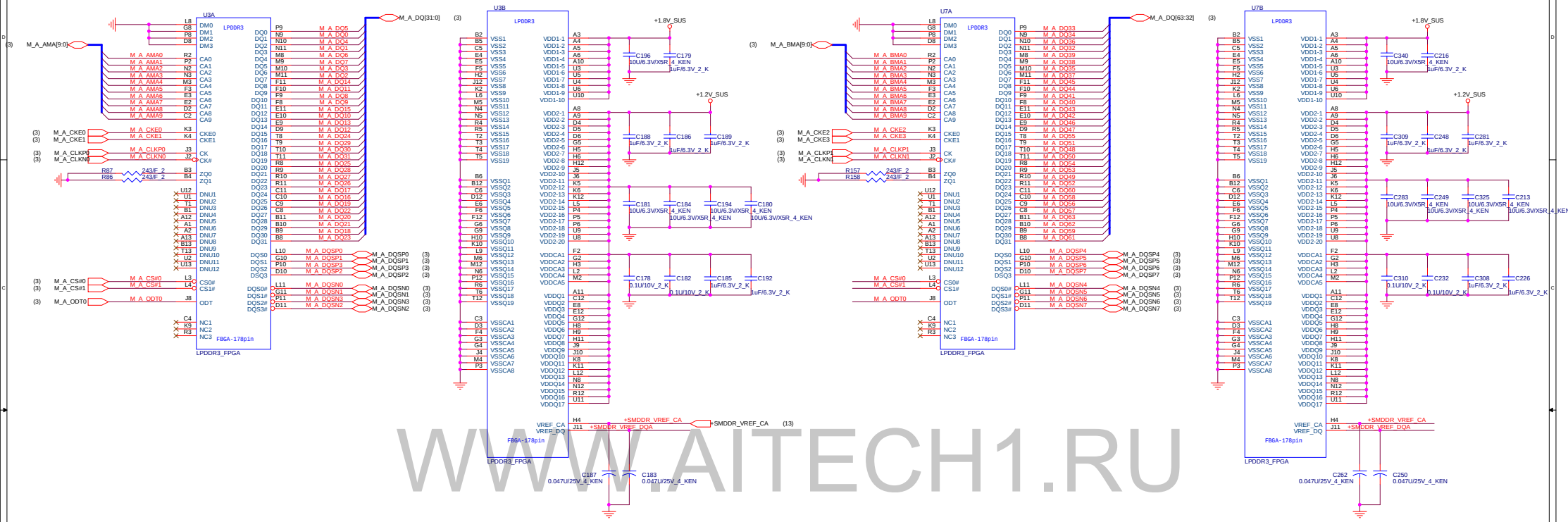
Processor Strapping

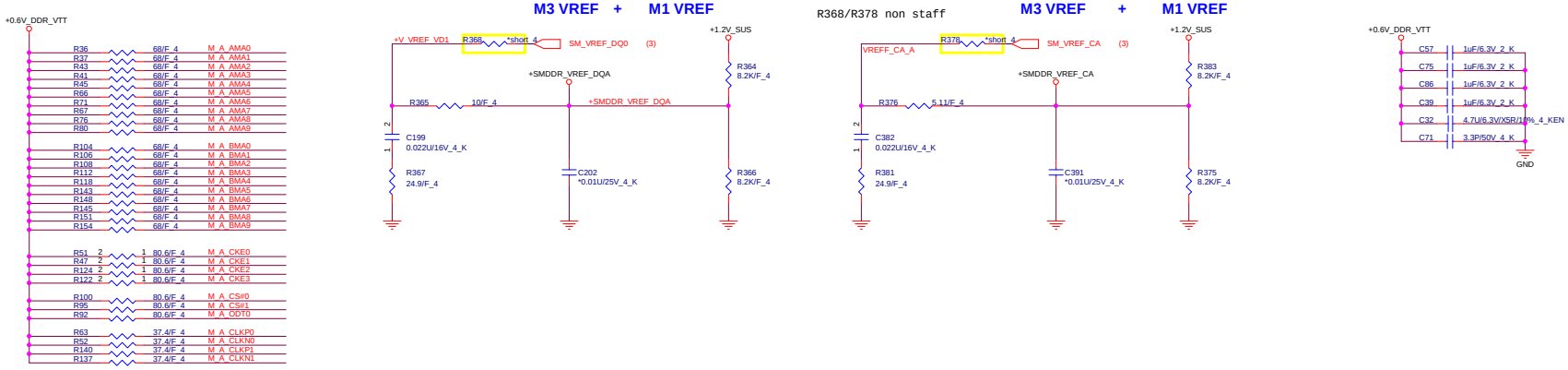
	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION NO STALL		CFG0 R54 *1K/F_2
CFG4 eDP Enable	DISABLED	ENABLED	CFG4 R53 1K/F_2
SPKR / GPP_B14	ENABLED	DISABLED	(5) ACZ_SPK R257 *1K/F_2 +3V
GSPI0_MOSI /GPP_B18	ENABLED	DISABLED	(5) NO_REBOOT R234 *1K/F_2 +3V
SMBALERT# /GPP_C2	ENABLED	DISABLED	Already Pull-high on Page.4
Boot BIOS Strap Bit /GPP_B22	LPC	SPI	(default:SPI) Page5 Reserve PU1K
SML0ALERT# / GPP_C5	ESPI	LPC	Already Pull-high on Page.4(default:LPC)
SML1ALERT# / PCHHOT#/ GPP_B23			Already Pull-high on Page.4
SPI0_MOSI (PCH_SPI_SI)			Already Pull-high on Page.4
SPI0_MISO (PCH_SPI_SO)			Already Pull-high on Page.4
SPI0_IO2 (PCH_SPI_IO2)			Already Pull-high on Page.4
SPI0_IO3 (PCH_SPI_IO3)			Already Pull-high on Page.4
HDA_SDO/ I2S_TXD0	DISABLED	ENABLED	Already Pull-high on Page.5
Security Flash Descriptors			
DDPB_CTRLDATA / GPP_E19	ENABLED		Used on HDMI DDC
DDPC_CTRLDATA / GPP_E21			No Used

Quanta Computer Inc.
PROJECT : NN5

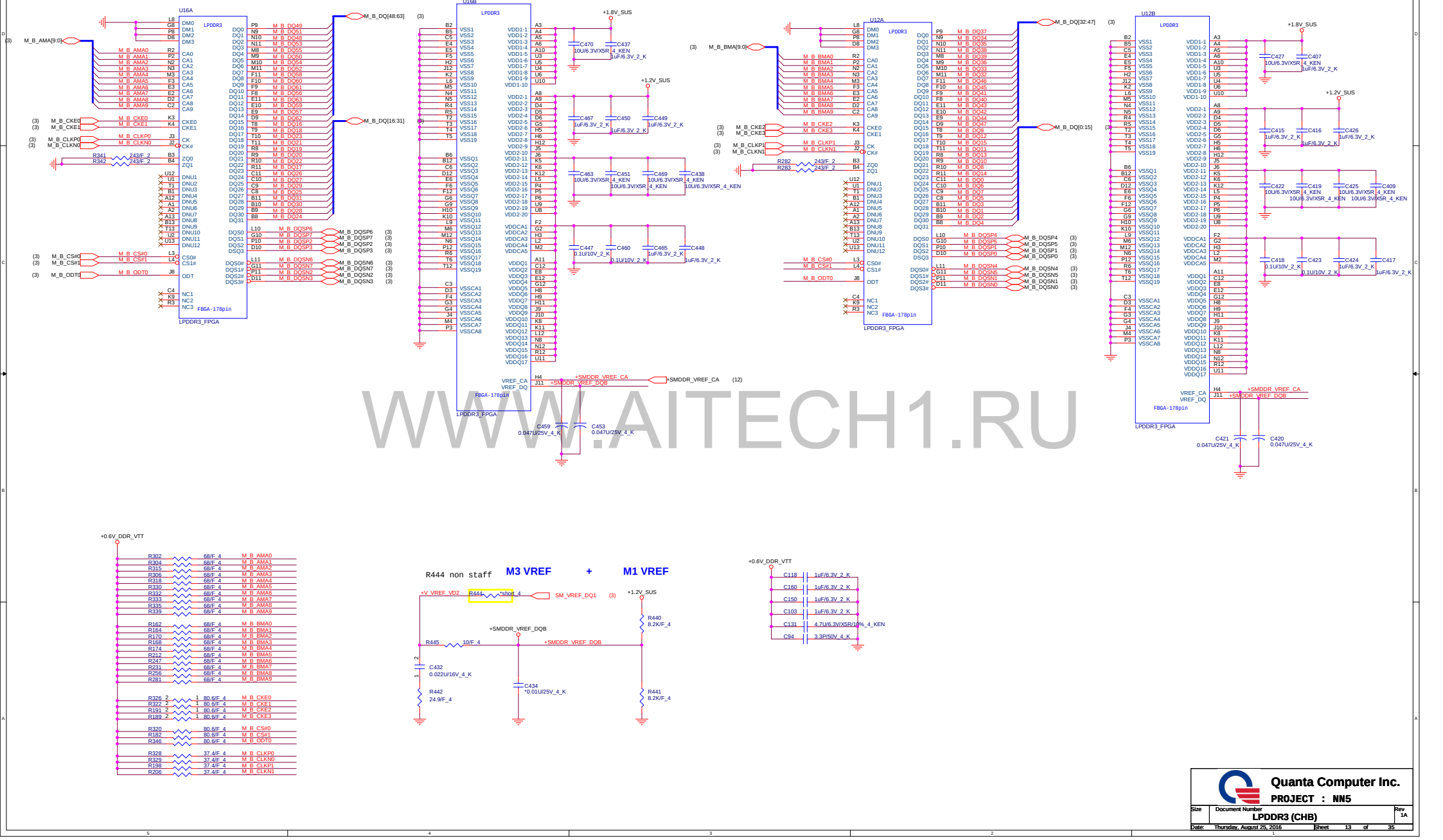
Size	Document Number	Rev
	SKL-Y CPU (VSS/CFG/RSVD)	1A

Date: Thursday, August 25, 2016 Sheet 11 of 35





Quanta Computer Inc.			
PROJECT : NN5			
Size	Document Number		Rev
	LPDDR3 (CHA)		1A
Date: Thursday, August 25, 2016	Sheet 12	of 35	



Quanta Computer Inc.

PROJECT : NN5

Size	Document Number	Rev
	LPDDR3 (CHB)	1A

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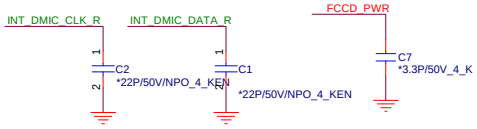
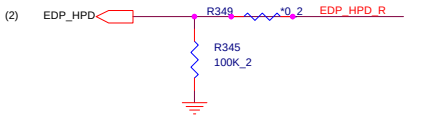
Camera

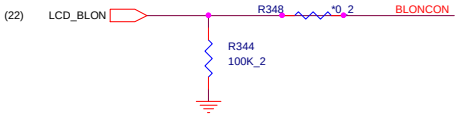
For EMI close to connector

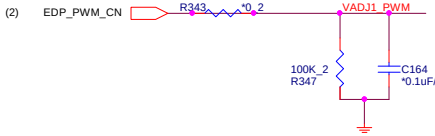
CLOSE to CN6

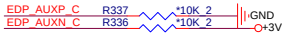


eDP





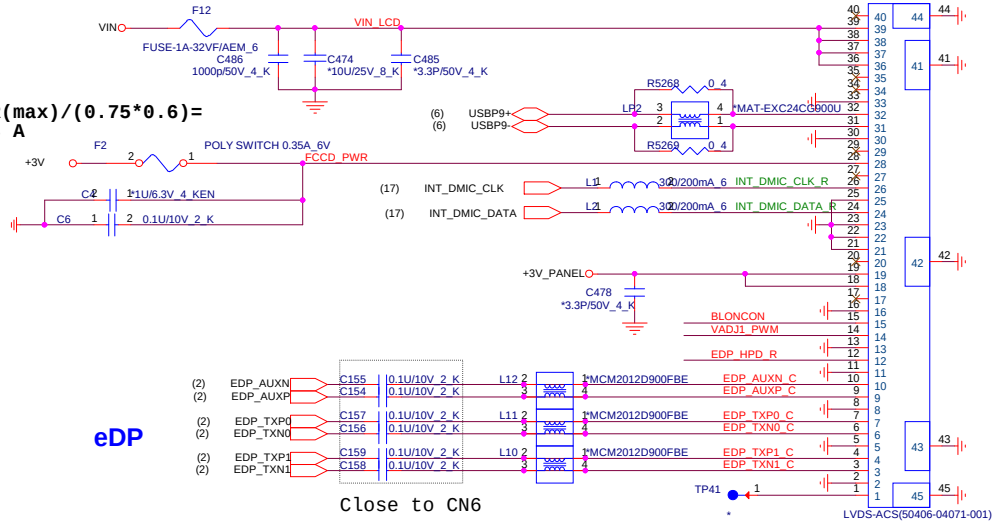




Fuse Rating= IR(max)/(0.75*0.88)=
0.251/0.66=0.383 A

Fuse Rating= IR(max)/(0.75*0.6)=
0.15/0.45=0.333 A

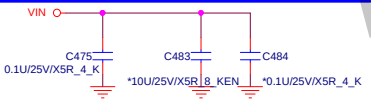
Camera

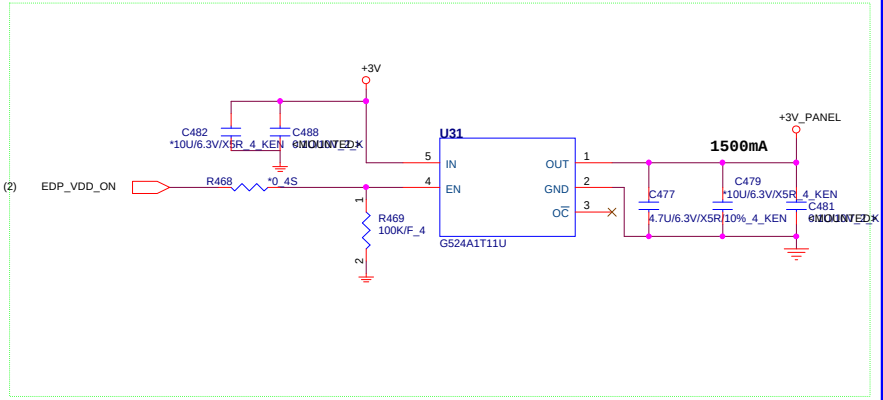


eDP

Close to CN6

LCD PWR

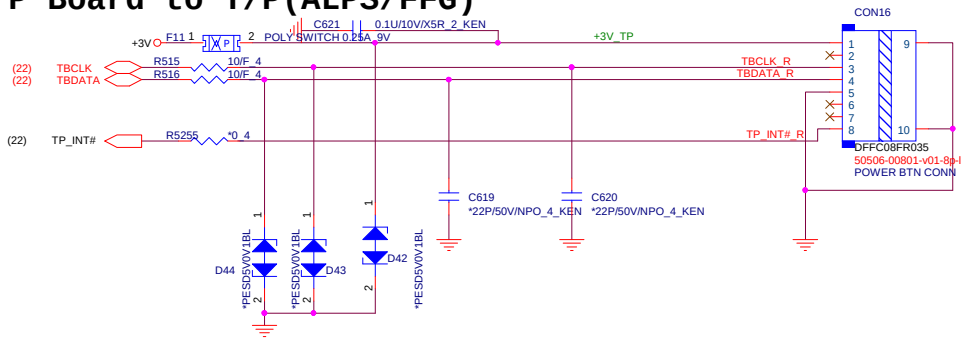




TOUCH PAD

Fuse Rating= IR(max)/(0.75*0.6)=
0.01/0.45= 0.022A

T/P Board to T/P(ALPS/FFG)



Quanta Computer Inc.		
PROJECT : NN5		
Size	Document Number: eDP/Touch PAD	Rev: 1A
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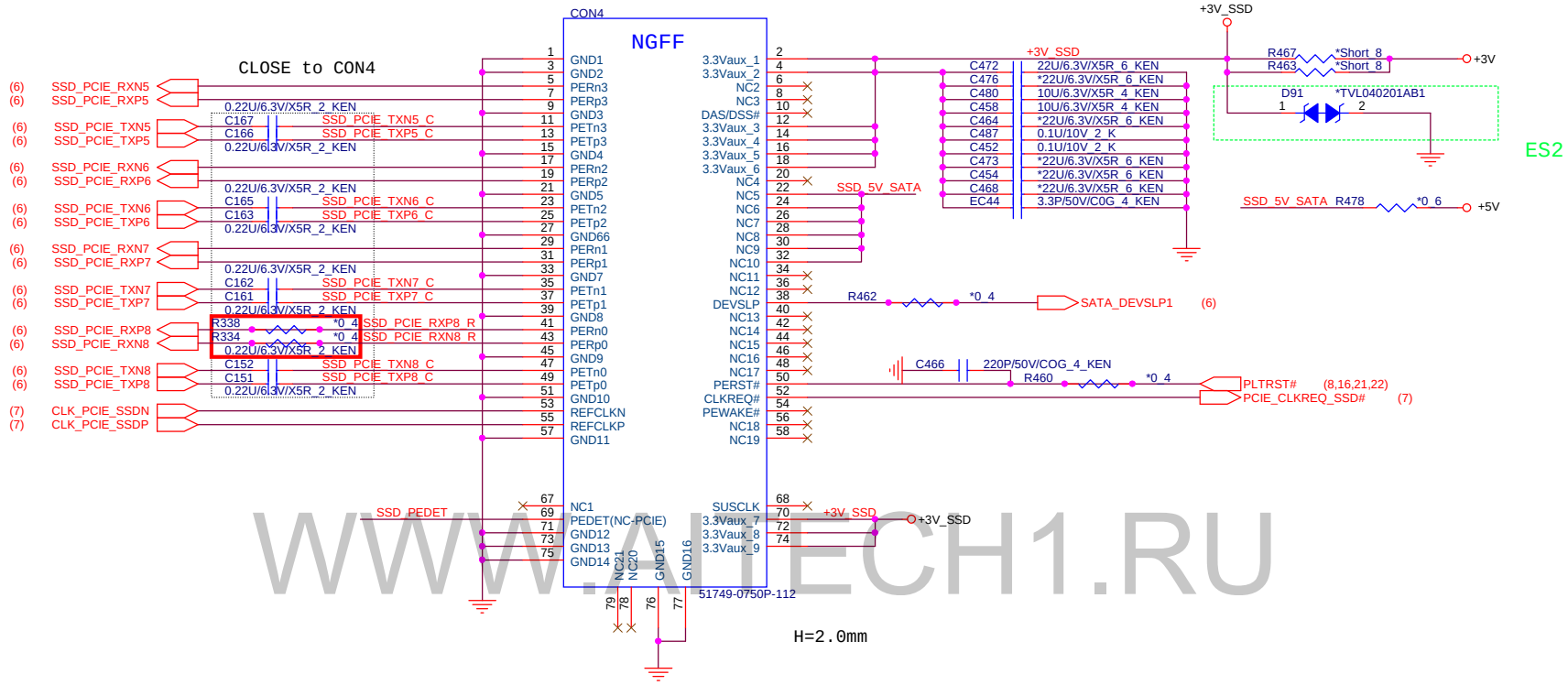
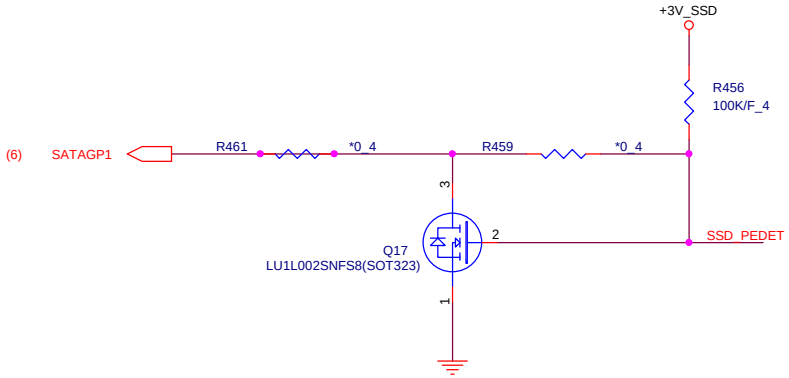
Peak
Current：2.0A,120mil

15

SSD CONNECTOR (Type M)



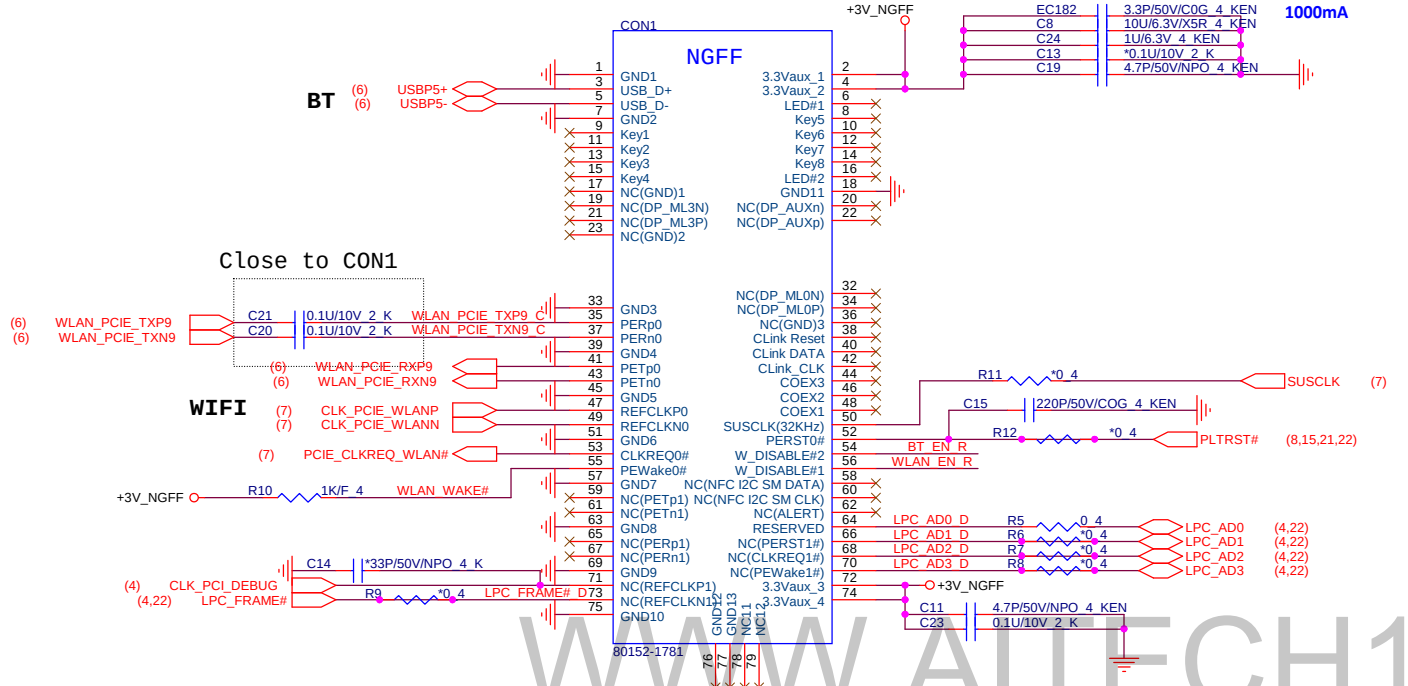


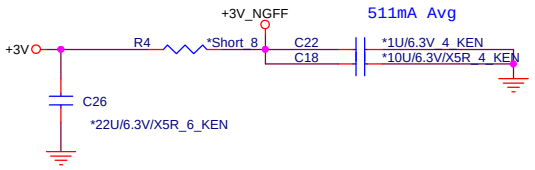
Quanta Computer Inc.
PROJECT : NN5

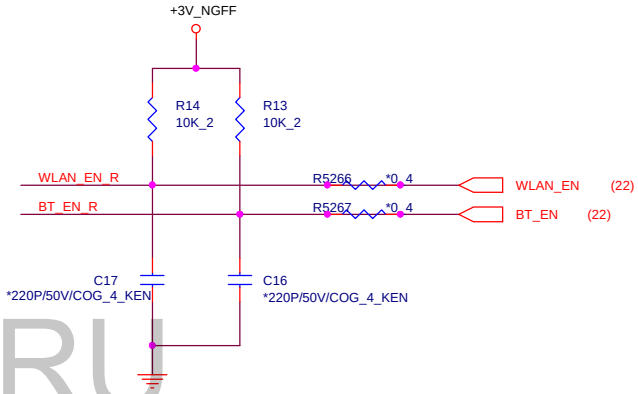
Size	Document Number	Rev
	SSD (NGFF CONN)	1A
Date: Thursday, August 25, 2016	Sheet 15 of 35	

NGFF Wifi/BT (Type E)

+3.3V_
NGFF_WLAN
Max Current :
1000mA







Quanta Computer Inc.
PROJECT : NN5

Size	Document Number	Rev
	WIFI/BT(NGFF)	1A
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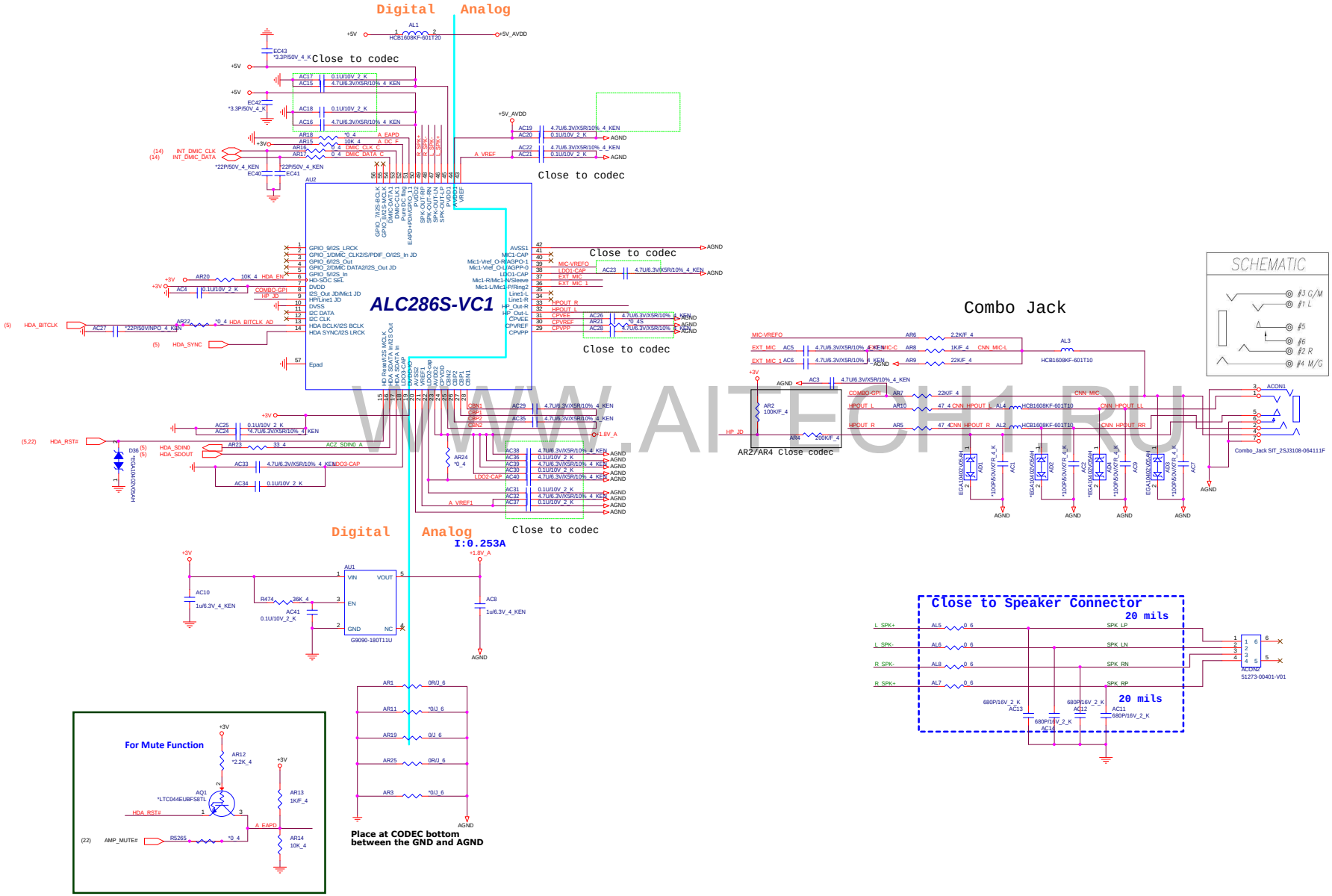
AUDIO(ALC286S-VC1)

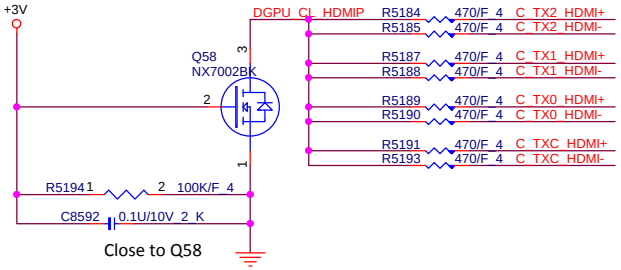


HDMI

Note:

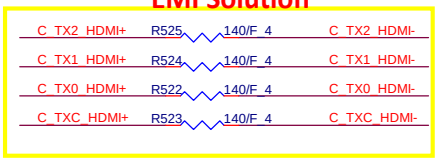
TX0 and TX2 lanes are swapped intentionally

PP modify 0905

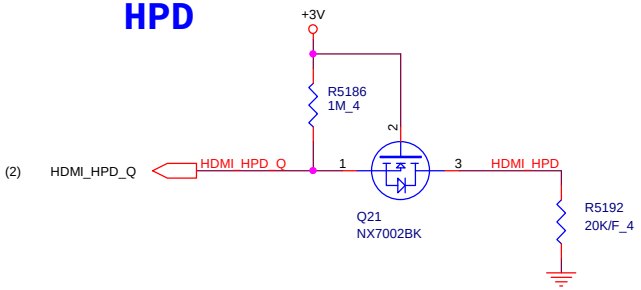


EMI

EMI Solution

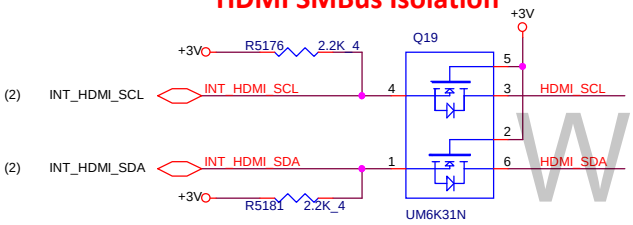


HPD



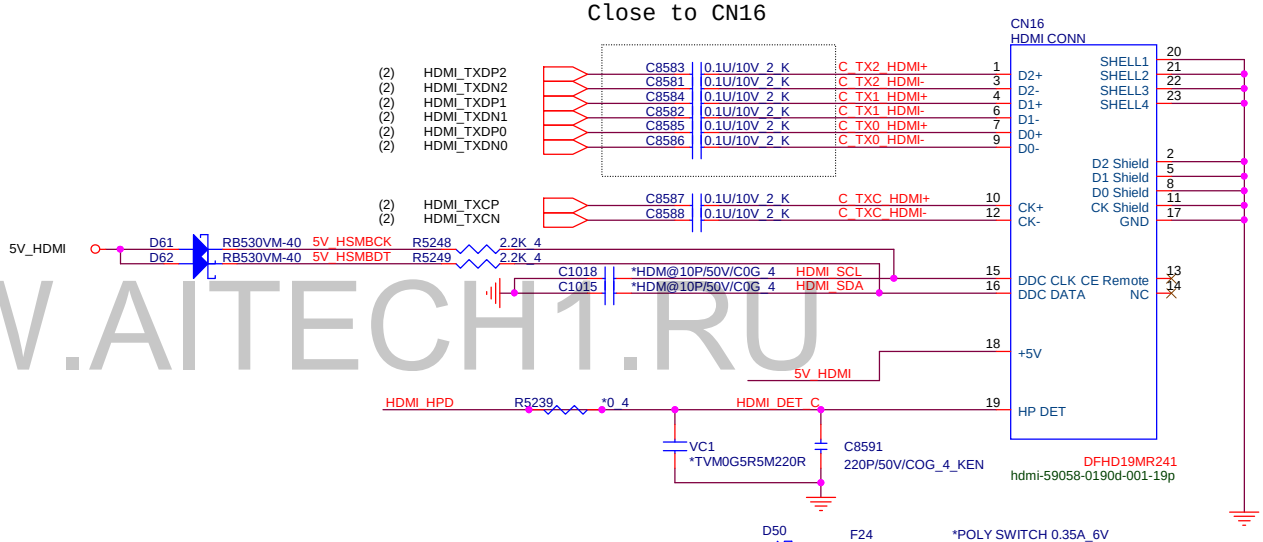
DDC Level Shift

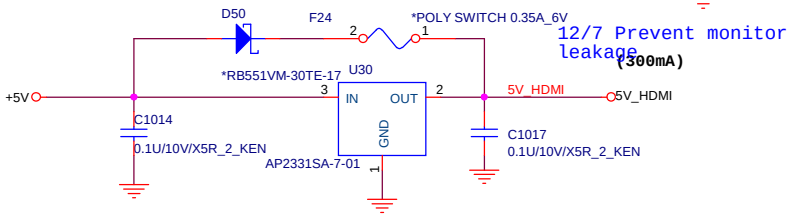
HDMI SMBus Isolation



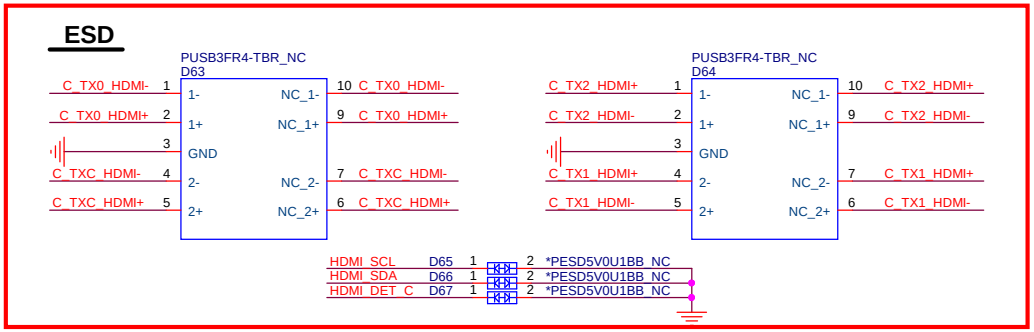
Close to HDMI connector

Close to CN16





ESD

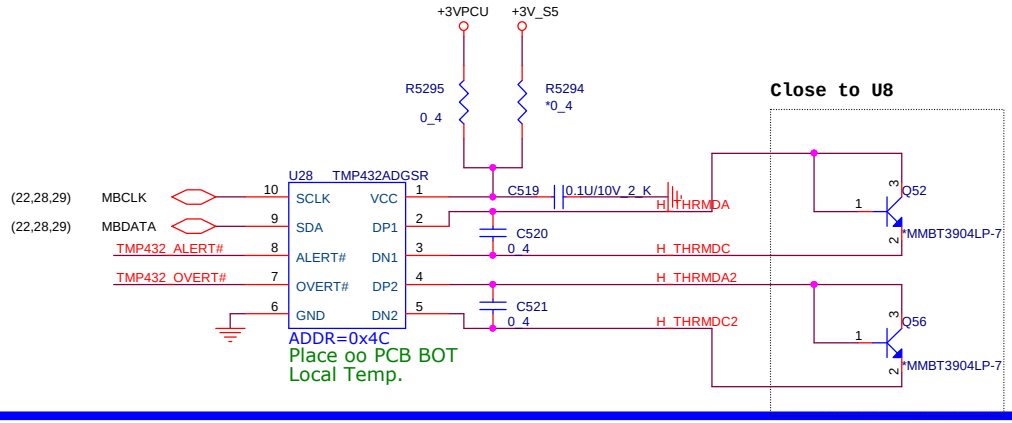


Quanta Computer Inc.

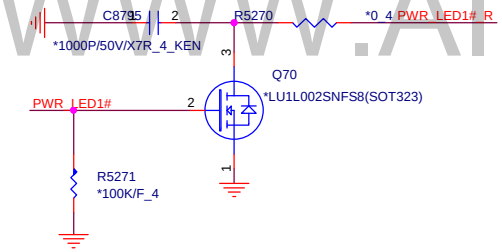
PROJECT : NN5

Size	Document Number	Rev
	HDMI	1A
Date: Thursday, August 25, 2016	Sheet 18 of 35	

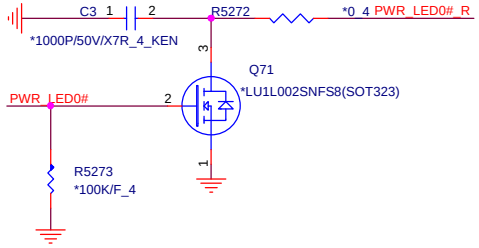
Thermal Sensor(THM)



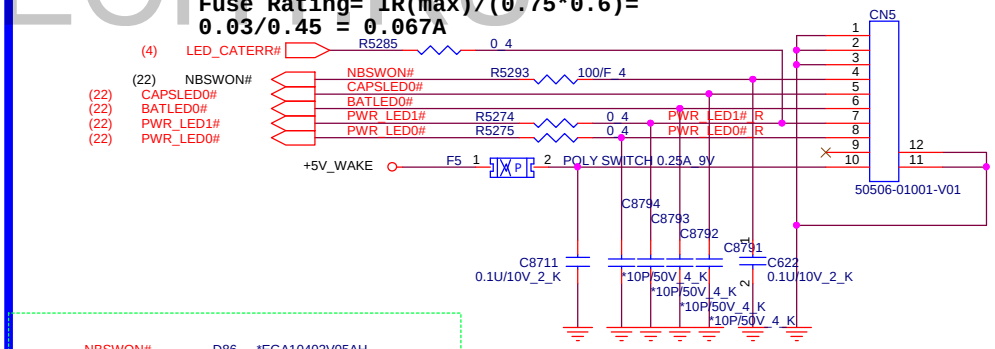
High Active(for reserved)

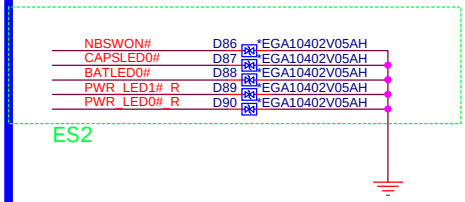


High Active(for reserved)



Fuse Rating= IR(max)/(0.75*0.6)=
0.03/0.45 = 0.067A

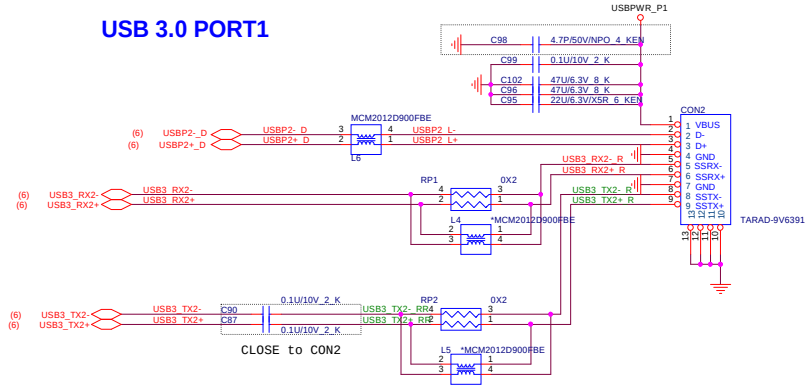


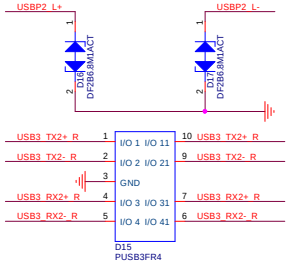


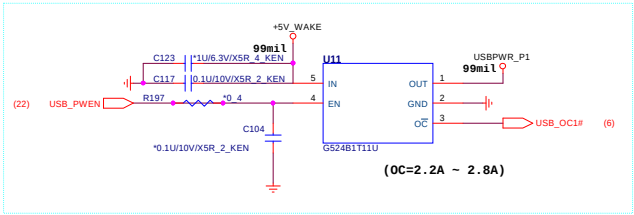
Quanta Computer Inc.
PROJECT : NN5

Size	Document Number	Rev
	BTB	1A
Date: Thursday, August 25, 2016	Sheet 19 of 35	

USB 3.0 PORT1

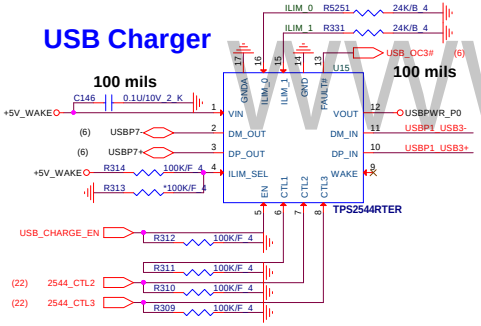


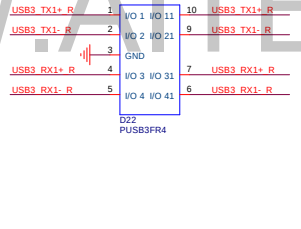


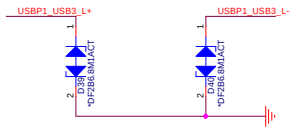


SEL	/OE	Mode
HIGH	LOW	USB Mode
LOW	LOW	UART Mode

USB Charger

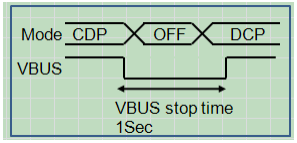






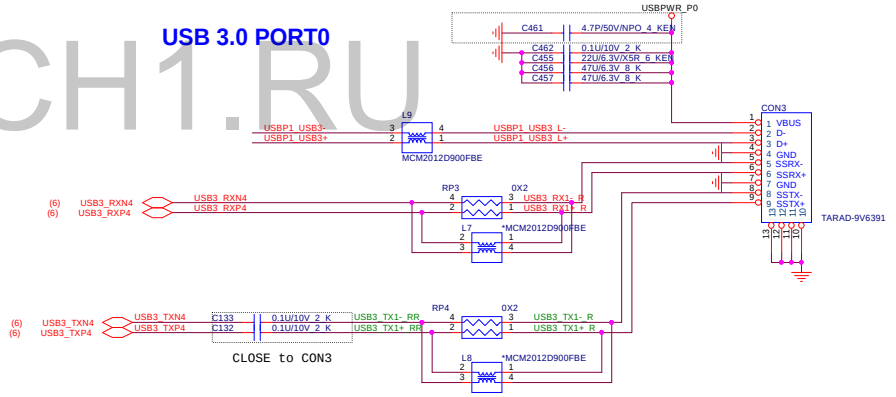
	TPS2541		TPS2544	
ILIM_SEL	Pin15	Pin16	Pin15	Pin16
High	V			V
Low		V	V	

SDP : Standard Downstream Port
CDP : Charging downstream port
DCP : Dedicated Charging Port
Enable/Disable : setting by EC



ILIM_SEL		(I LIMIT(A)= 50250/R)
HI	I_LIM_1	50250/24K=2.093A
LO	I_LIM_0	50250/24K=2.093A

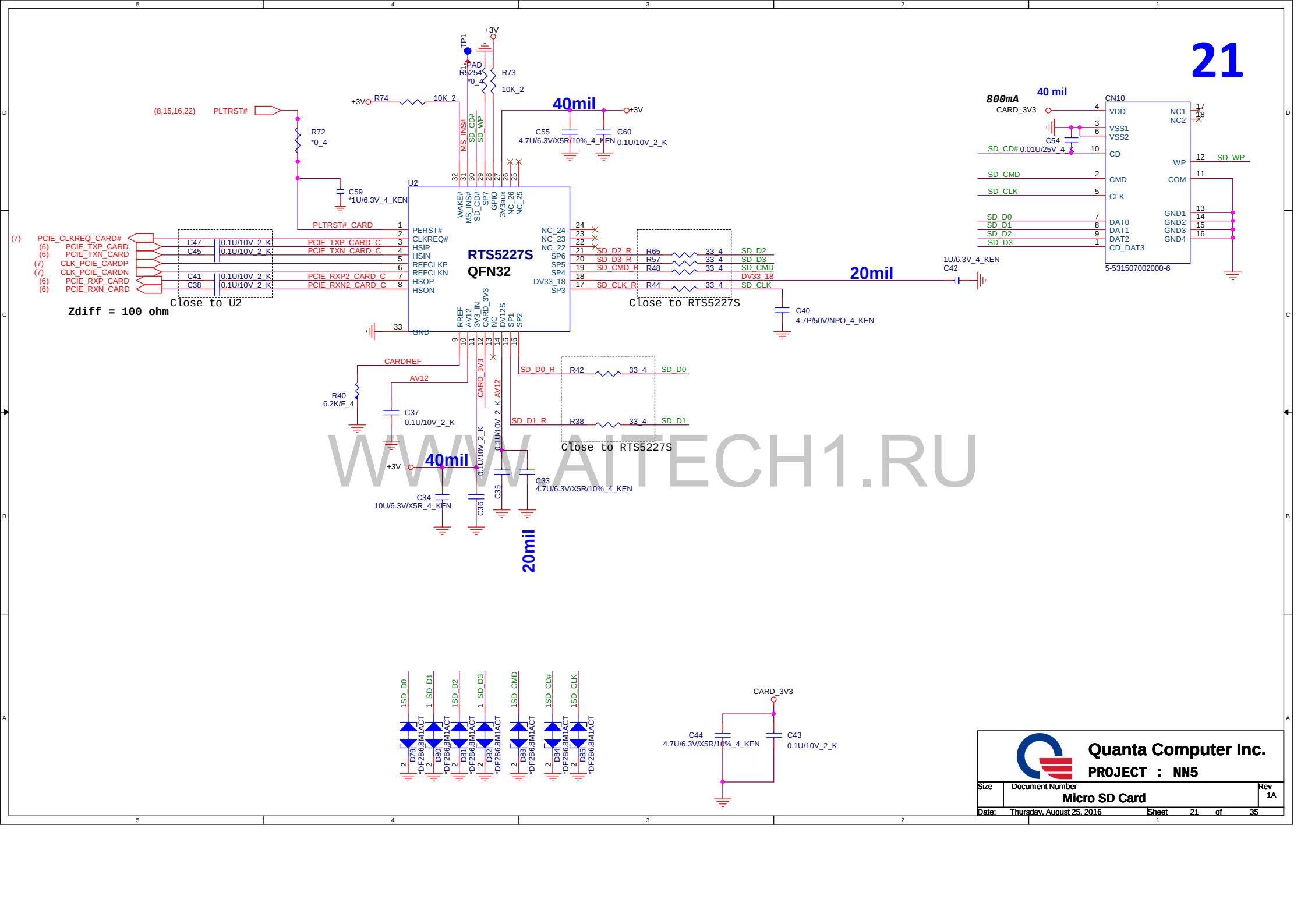
USB 3.0 PORT0



USB_CHARGE_EN	CTL_1	CTL_2	CTL_3	TPS 2544 Truth Table
1	0	X	1	DCP,Auto-detect(S3/S4/S5, 1.5A)
1	1	0	0	DCP, BC SPEC1.2 only(S3/Deep standby/S4/S5, 1.5A)
1	1	0	1	DCP, Divider mode only(S3/S4/S5, 1.5A)
1	0	1	0	SDP, USB2.0 mode(S0, 0.5A)
1	1	1	1	CDP (S0, 1.5A)
0	0	0	0	OUT discharge, power switch OFF

System State	USB Battery Charging Setting		
	Disable(AC and DC mode)(EN1 2 3)	Enable(AC mode)(EN1 2 3)	Enable(DC mode)(EN1 2 3)
S0	SDP (1 0 1 0)	SDP (1 0 1 0)	SDP (1 0 1 0)
S3	SDP (1 0 1 0)	DCP Auto (1 0 X 1)	Charger OFF (0 0 0 0)
S4	Charger OFF (0 0 0 0)	DCP Auto (1 0 X 1)	Charger OFF (0 0 0 0)
S5	Charger OFF (0 0 0 0)	DCP Auto (1 0 X 1)	Charger OFF (0 0 0 0)

Quanta Computer Inc.
PROJECT : NN5
Size | Document Number: USB3.0/USB CHARGER | Rev 1A
Date: Thursday, August 25, 2016 | Sheet 20 of 35



Quanta Computer Inc.		
PROJECT : NN5		
Size	Document Number: Micro SD Card	Rev: 1A
Date: Thursday, August 25, 2016	Sheet 21 of 35	

EC IT8987

+3VPCU_EC and +3V_RTC
minimum trace width 12mils.

12 mils

EC change to VFBGA Package
PN is AL008987T00

(For PLL Power)

IT8987
VFBGA

LPC
GPIO
SM BUS
PS/2
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
A/D D/A
KBMX
CLOCK

For Battery/Thermal Sensor
For PCH SMB Thermal

ES2

Add KR82 for tPCH10

Add KR81 for tPCH10

Add KR79 for tPCH10

Reserve for ESD

22

EC PU/PD

ES2

R127,R5280 for share ROM, non-staff when Mount EC ROM

Put damping resistor close to EC
Close to EC

2/23 Correct description to W25Q80DVSSIG

KEY BOARD Connector

CON7
51653-02401-V01

LID SENSOR

For throttling

HALL SENSOR

HE1
APX8132AI-TRG

ALL_SYS_PWRGD >10ms
EC_PWROK
99ms
PCH_PWROK_EC

FFG-->Reserved

Add 3 AND GATEs reserve for tPCH10

Quanta Computer Inc.
PROJECT : NN5
KBC IT8987
Size: Document Number: Rev 1A
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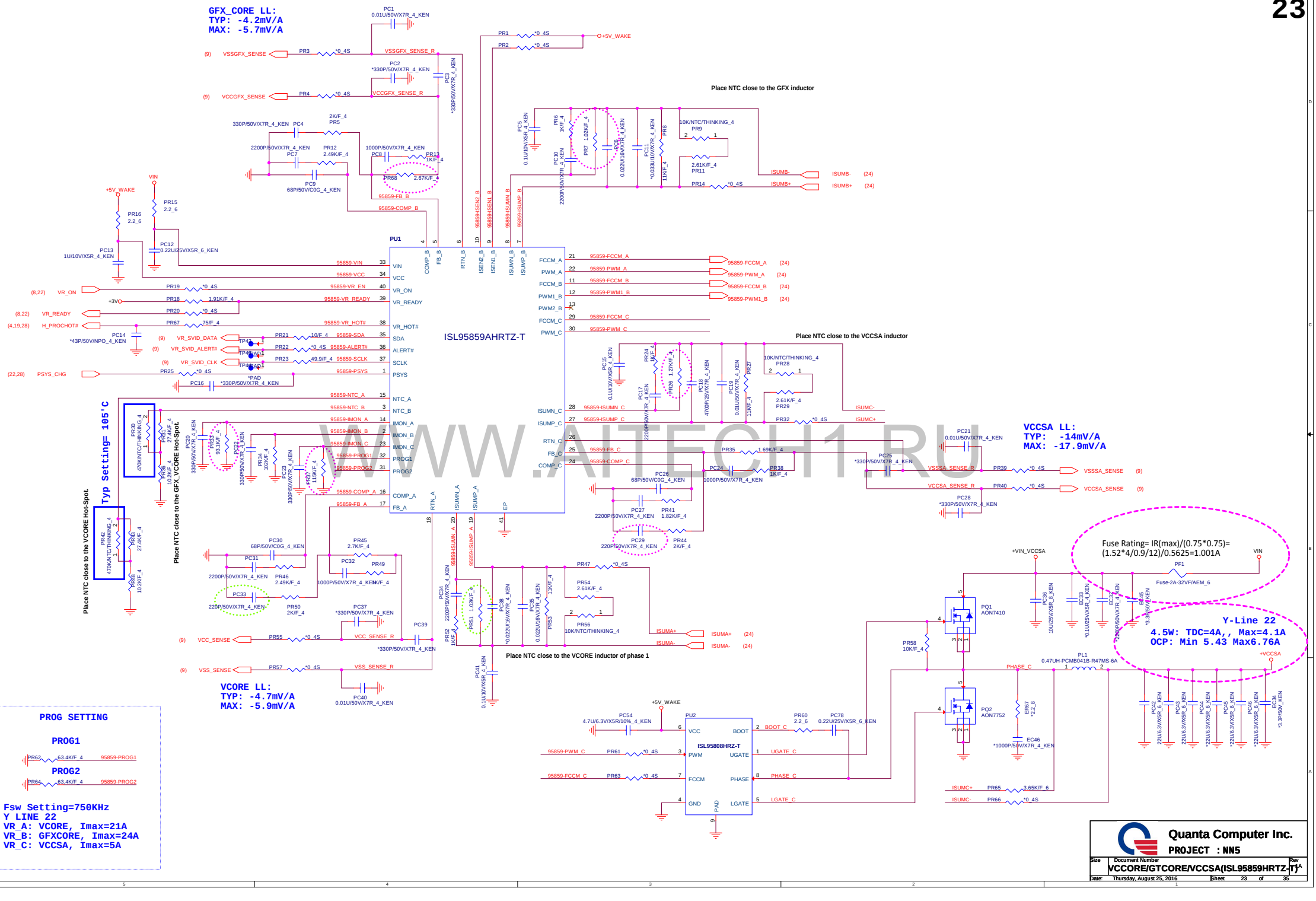

Quanta Computer Inc.
PROJECT : NN5

Size	Document Number	Rev
	VCCORE/GTCORE/VCCSA(ISL95859HRTZ-T)	1A

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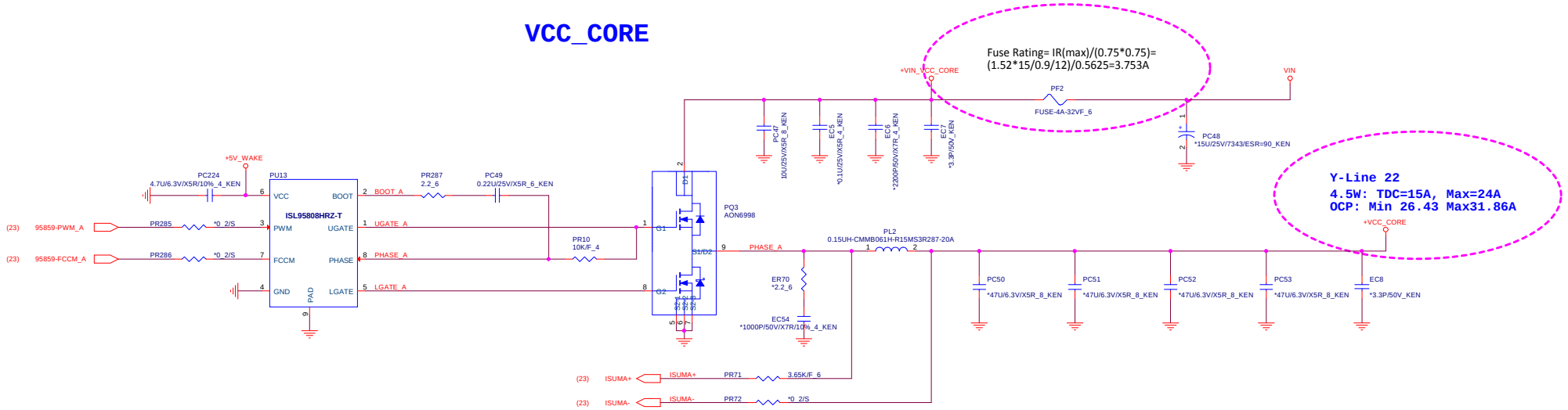
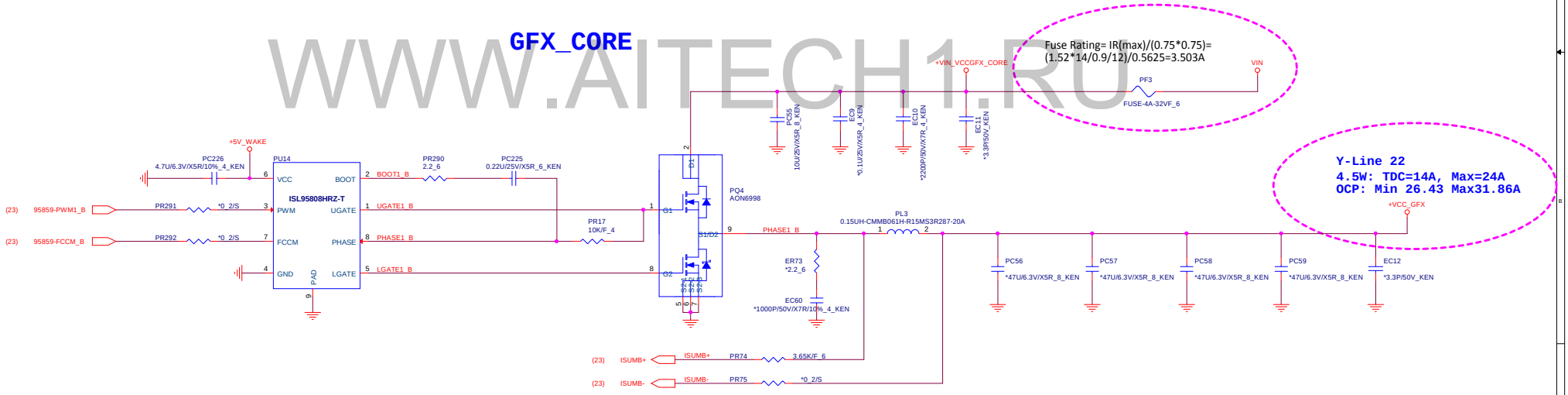
VCC_CORE



GFX_CORE



Quanta Computer Inc.
PROJECT : NN5

Size	Document Number	Rev
	VCCORE/GTCORE/VCCSA (ISL95859HRTZ-T)	
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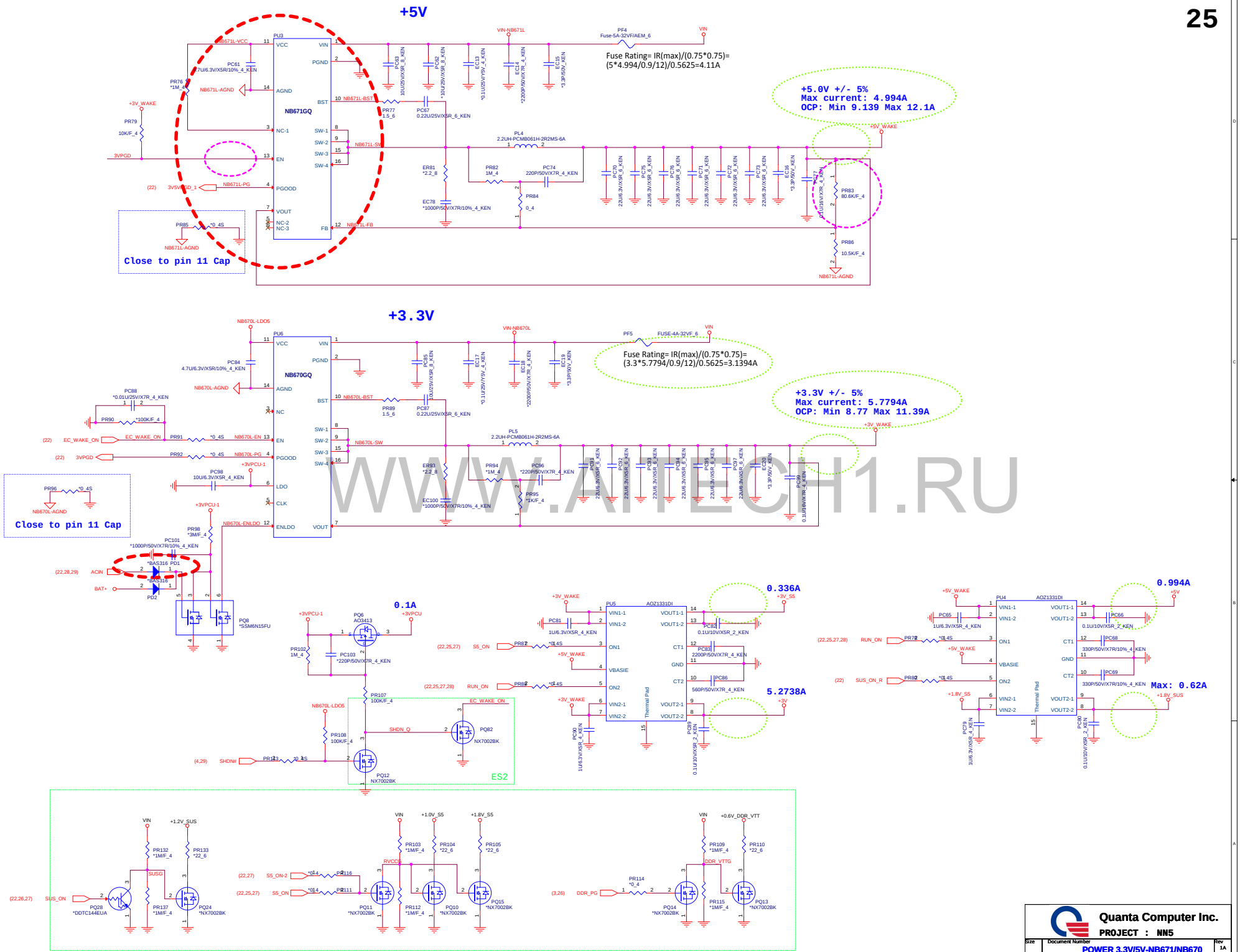

Quanta Computer Inc.
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Size | Document Number: POWER 3.3V/5V-NB671/NB670 | Rev 1A
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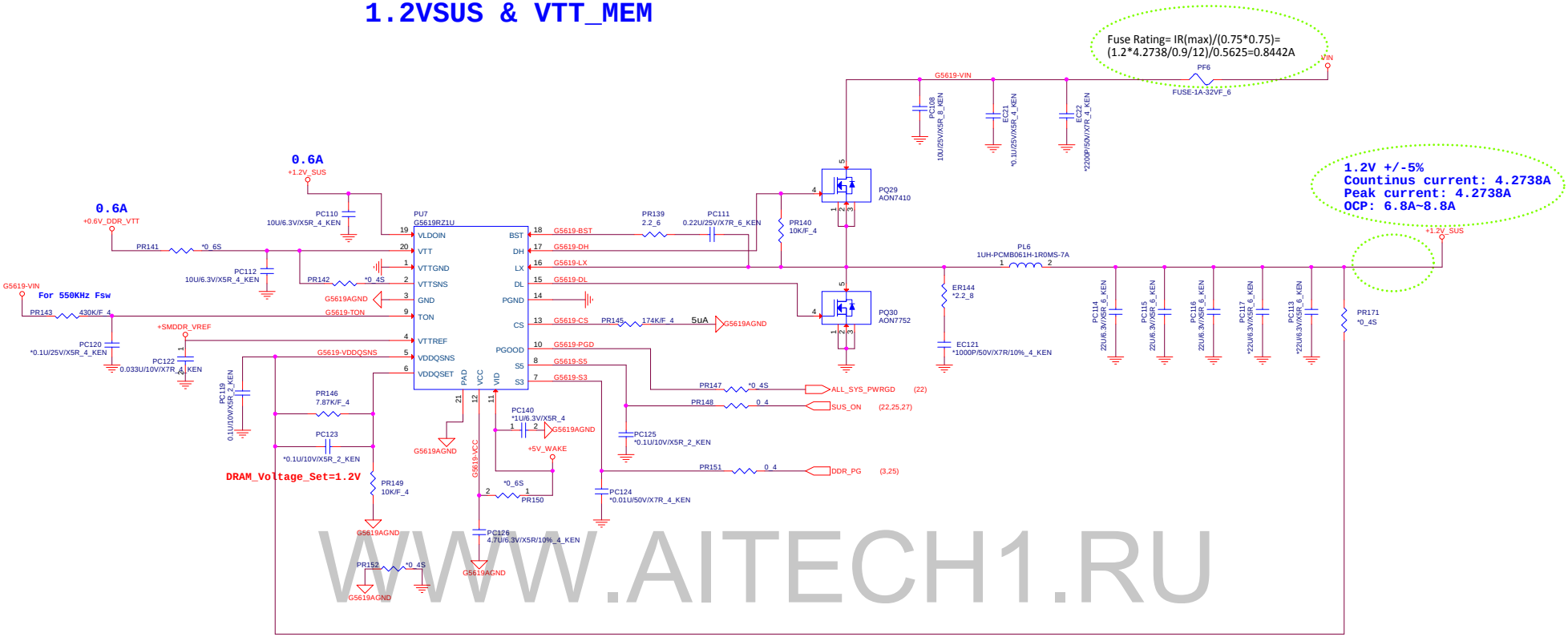
1.2VSUS & VTT_MEM



STATE	S3	S5	1.35VSUS	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	Off/High Z
S4/S5	0	0	Off	Off	Off

Quanta Computer Inc.
PROJECT : NN5

Size	Document Number	Rev
	1.2VSUS/VTT_MEM	1A

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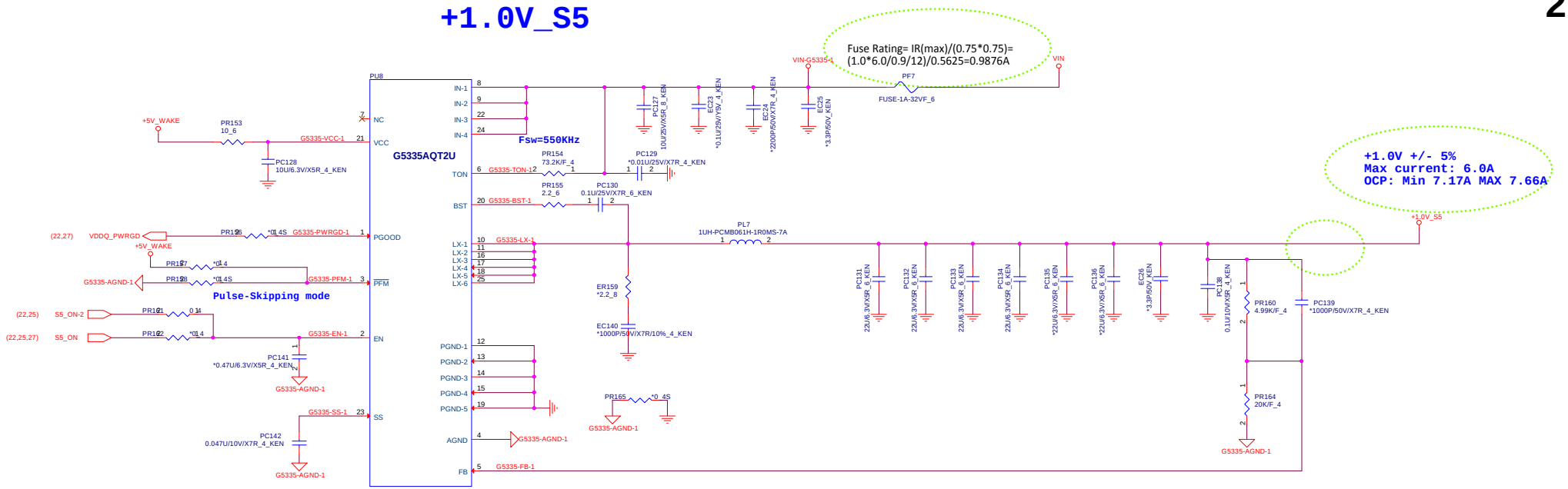
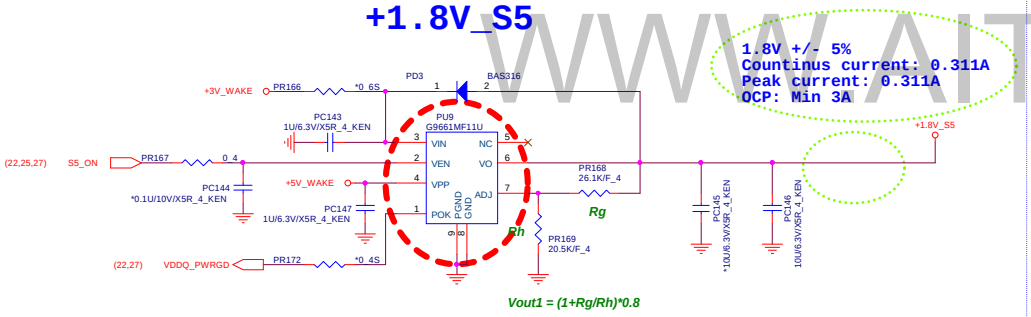
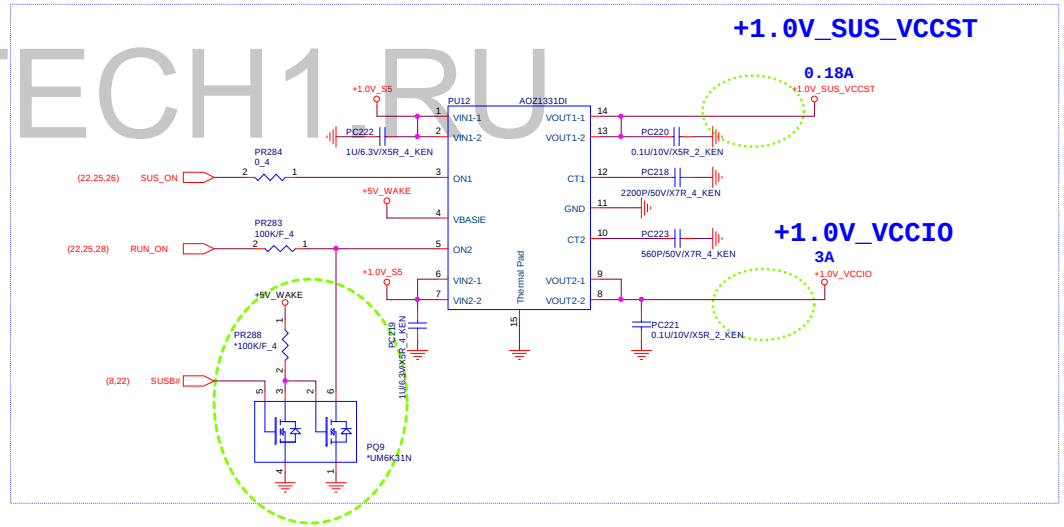
+1.0V_S5



+1.8V_S5



+1.0V_SUS_VCCST



Quanta Computer Inc.
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Size	Document Number	Rev
	+1.0V_S5 / +1.8V_S5 / +1.8V	1A

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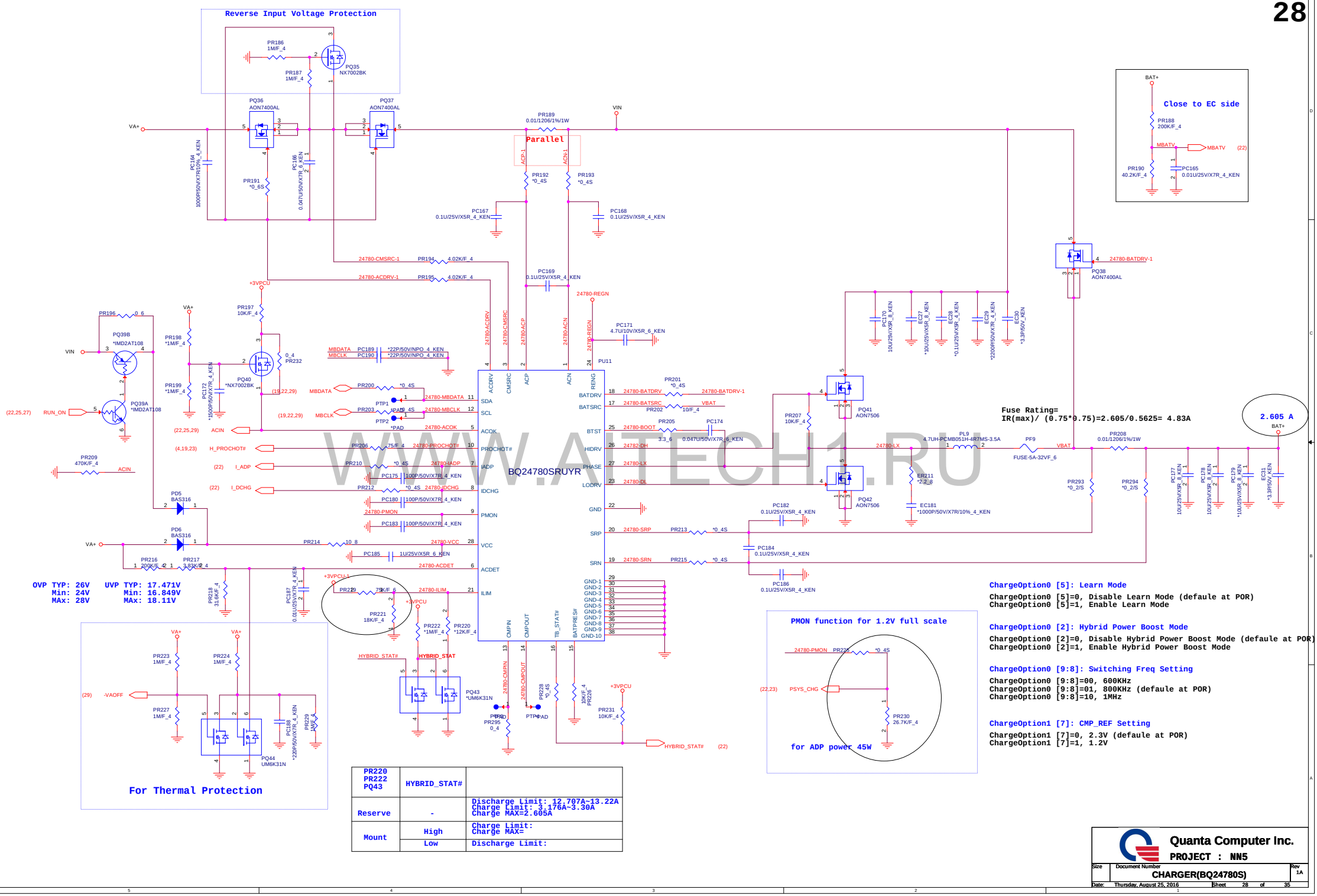
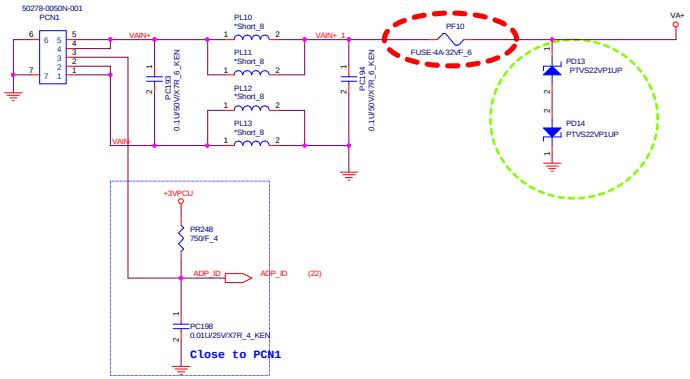


AC IN

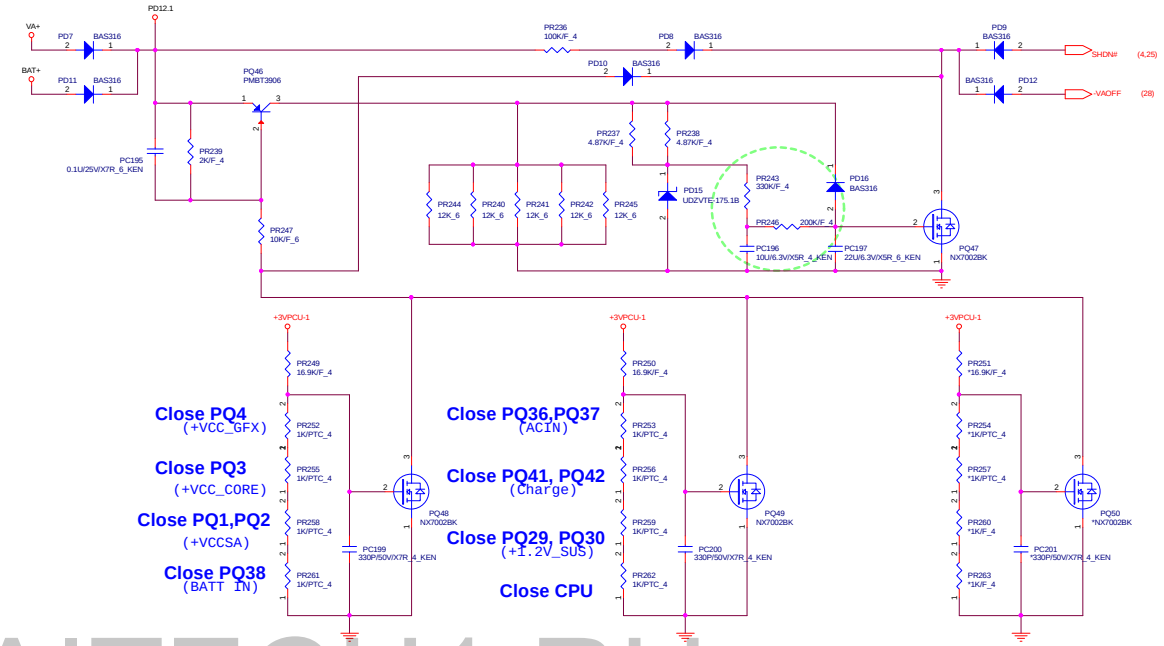
AC ADAPTOR IN CONN

P/N & Footprint

Fuse Rating=
IR(max)/ (0.75*0.75)=2.25/0.5625= 4A



Thermal Protection



Close PQ4 (+VCC_GFX)

Close PQ3 (+VCC_CORE)

Close PQ1,PQ2 (+VCCSA)

Close PQ38 (BATT IN)

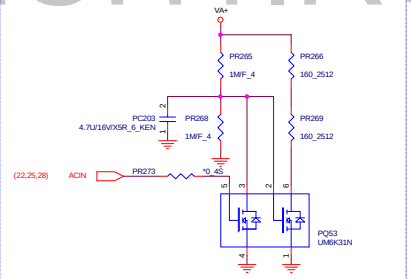
Close PQ36,PQ37 (ACIN)

Close PQ41, PQ42 (Charge)

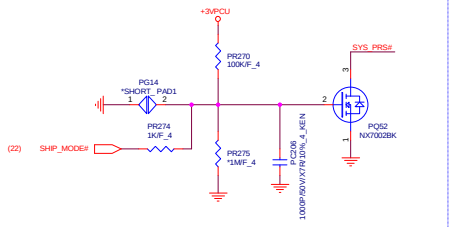
Close PQ29, PQ30 (+1.2V_SUS)

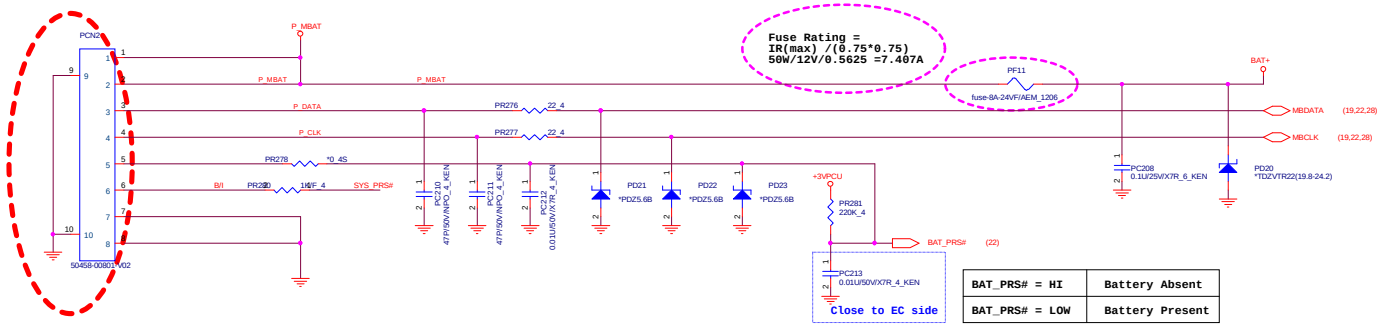
Close CPU

Adapter Discharge



Shipping Mode





BAT_PRS# = HI	Battery Absent
BAT_PRS# = LOW	Battery Present

Quanta Computer Inc.
PROJECT : NN5

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	ADP IN / BAT IN / Thermal Protection	1A

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SCREW HOLE

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CPU HOLE

H2 *H-NN5-TB1
H4 *H-NN5-TB2
H5 *h-c217d138p2
H6 *h-tbc217c178d138p2
H10 *h-c217d138p2
H11 *h-c217d138p2
H12 *H-R208X305
H13 *H-TIC217BC256D91P2

PAD

H14 *H-CT217SB256D91P2
H18 *H-O95X83D95X83N
H19 *H-CT118B197D83X95
H20 *H-TIC118BC177D83P2

PAD21 *SPAD-NN5-1
PAD36 *SPAD-NN5-1
PAD24 *SPAD-NN5-3
PAD25 *SPAD-NN5-3

For ESD's requirment

PAD23 *S-NN5-5TT
PAD26 *SPAD-NN5-4

GND

CLIP SHIELDING(CPU)

35

PAD1 *FBYB1001010
PAD2 *FBYB1001010
PAD7 *FBYB1001010
PAD8 *FBYB1001010
PAD10 *FBYB1001010

GND

+3V_WAKE

C8799 *0.1U/10V/X5R_2_XEN
C8800 *0.1U/10V/X5R_2_XEN
C8801 *0.1U/10V/X5R_2_XEN
C8802 *0.1U/10V/X5R_2_XEN
C8803 *0.1U/10V/X5R_2_XEN

GND

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Size	Document Number	Rev
	SCREW/DEBUG/80 PORT/Ship	1A

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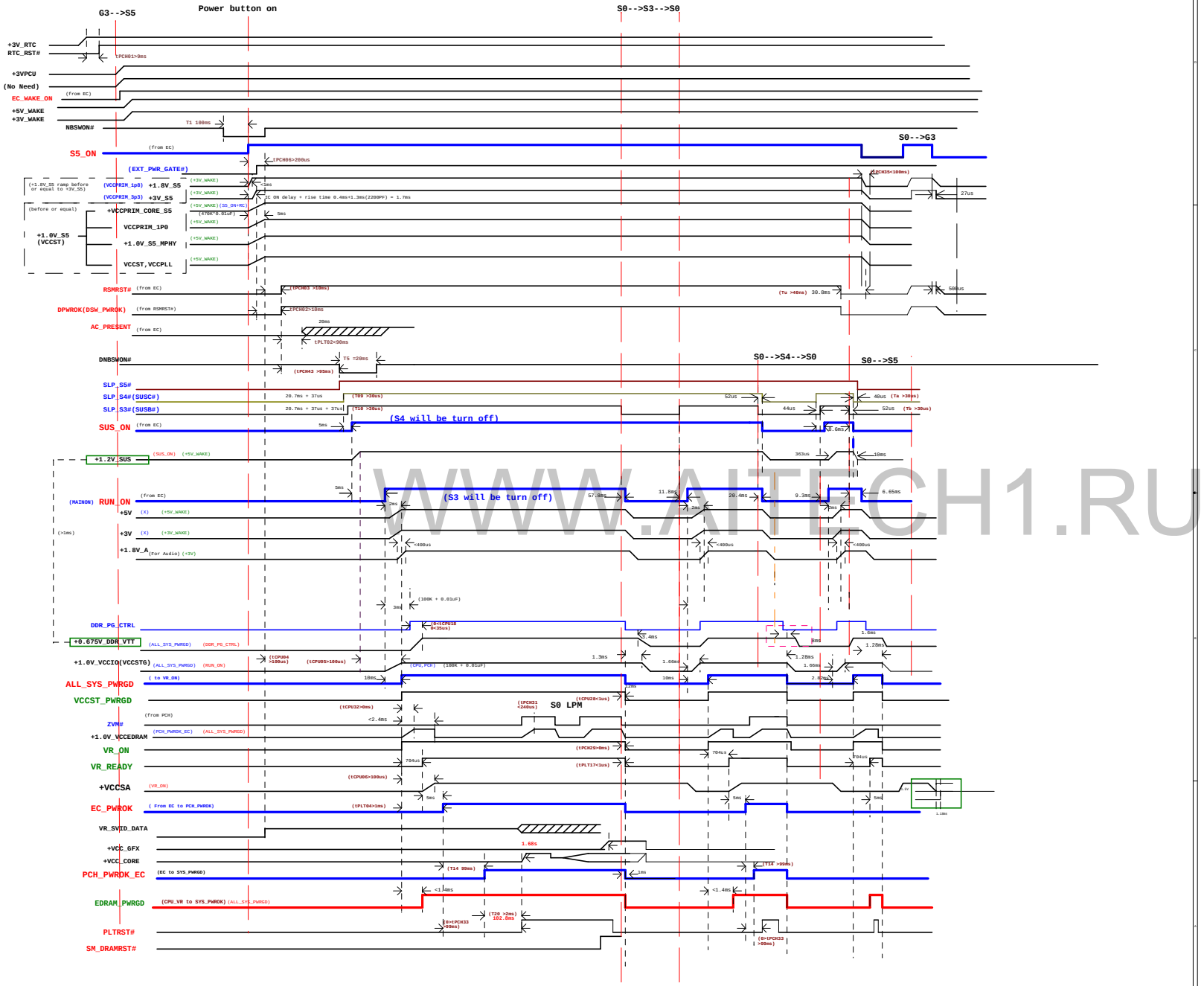
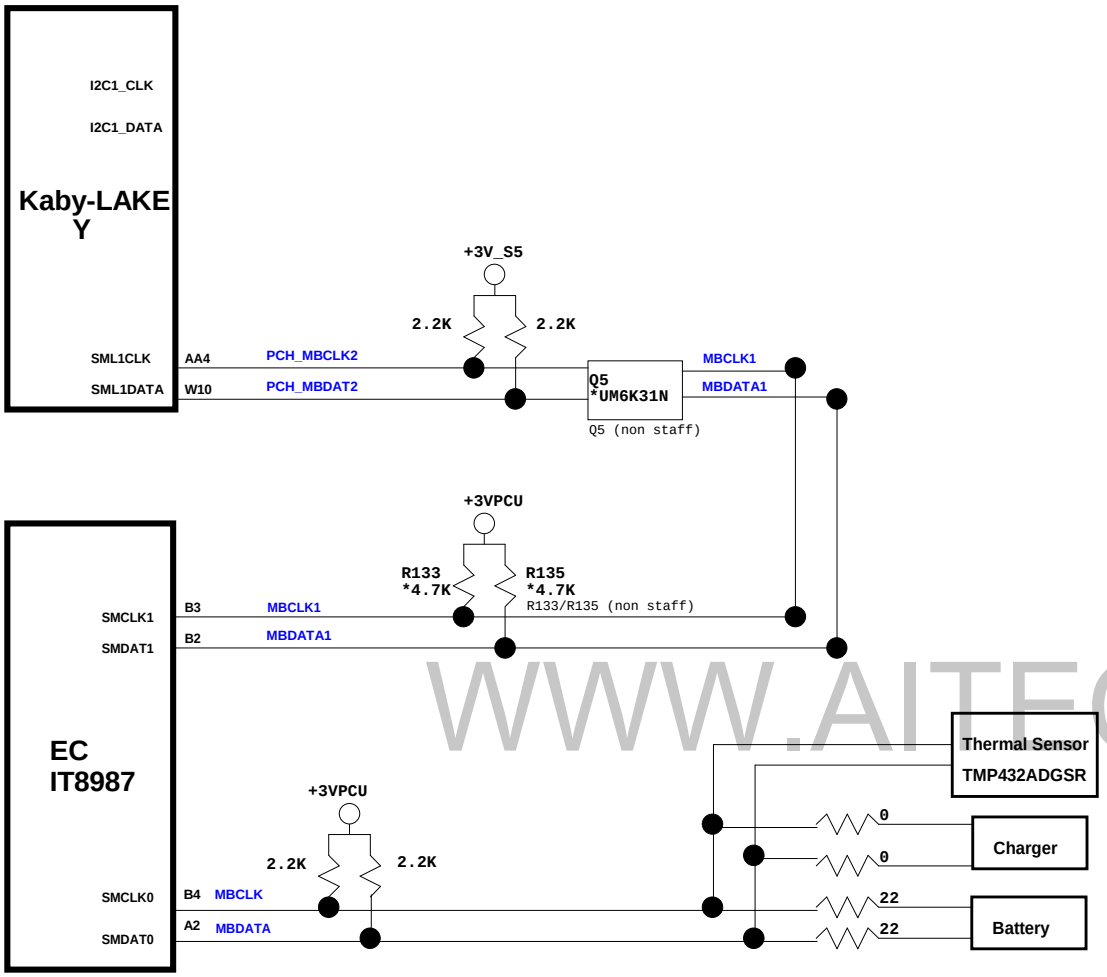
SkyLake U/Y Power-Up Sequencing (G3-->S0-->S3-->S4-->S5)



Quanta Computer Inc.
PROJECT : MN5
Power Sequence



Quanta Computer Inc.
PROJECT : NN5
Size | Document Number: I2C Block diagram | Rev 1A
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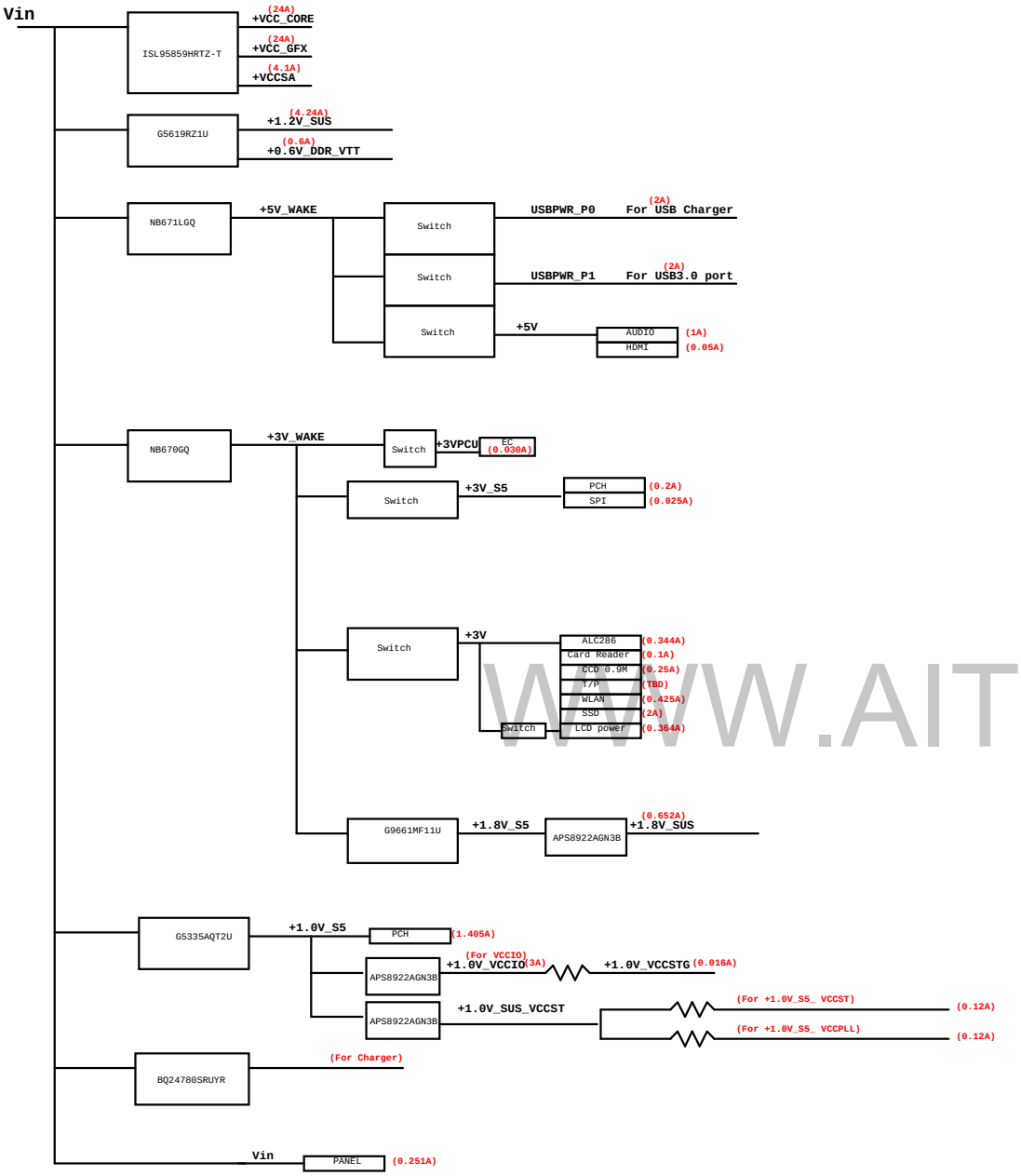

Quanta Computer Inc.
PROJECT : NN5
Power Diagram
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OS status	S0	S3	(Soft OFF)	(Soft OFF)
H/W status	S0	S3	S5 S4 (Win10 off) Charge Enable	S5 S4 (Win10 off) Charge Disable
RUN_ON	H	L	L	L
+3V	H	L	L	L
+5V	H	L	L	L
+0.6V_DDR_VTT	H	L	L	L
+1.8V_A	H	L	L	L
+VCCSA	H	L	L	L
+VCC_GFX	H	L	L	L
+VCC_CORE	H	L	L	L
+1.0V_VCCIO(+1.0V_VCCSTG)	H	L	L	L
SUS_ON	H	H	L	L
+1.2V_SUS	H	H	L	L
+1.8V_SUS	H	H	L	L
+1.0V_SUS_VCCST	H	H	L	L
S5_ON	H	H	L	L
+1.8V_S5	H	H	L	L
+3V_S5	H	H	L	L
+1.0V_S5	H	H	L	L
EC_WAKE_ON	H	H	H	L
+3V_WAKE	H	H	H	L
+5V_WAKE	H	H	H	L
+3VPCU-1	H	H	H	H
+3VPCU	H	H	H	H

Quanta Computer Inc.
PROJECT : NN5

Size	Document Number	Rev
	POWER MAP	1A
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CHANGE LIST ES1 to ES2

Page 22-- Add R5279 to inform EC the HDA_RST# status.
Page 07-- Remove R540 for reserve only.
Page 22-- Add R5280 to support EC e-flash function
Page 08-- de-mount R395,mount R5262 -->No support deep sleep
Page 21-- U1,U4 Change the ESD parts from U1,U4 to D79,D80,D81,D82,D83,D84,D85.
Page 25-- Add PQ82 to avoid SHDN# issue.
Page 22-- Reserved U32,C8797 to follow FFG.
Page 22-- Reserved Q73 for RTC measure.
Page 19-- Reserved D86~D90 for ESD.
Page 30-- Reserved C8799~C8803 for ESD.
Page 15-- Reserved D91 for ESD.
Page 25,26,27,29-- Del PG1~8,PG10,PG14~16
Page 4-- Add R5283,R5284,Q72 for CATERR# by NEC
Page 4-- Add R5285 for CATERR# by NEC.
Page 25-- PR83 change from 75K to 80.6K.
Page 23-- PF1 change from 1A to 2A.
Page 24-- PF2 change from 3A to 4A.
Page 24-- PF3 change from 3A to 4A.
Page 29-- PF11 change from 6A to 8A.
Page 29-- PR243 change from 301K to 330K.
Page 29-- PR246 change from 100K to 200K.
Page 4-- Add R5288 for CATERR# for Intel #563377_2016WW20.
Page 7-- R226 chang value from 2.7K +/-1% to 2.71K +/-0.5% for Intel #563377_2016WW18.
Page 22-- Add R5290,R5291,KC43,KC44 by NEC's require.
Page 10-- C511 change size from 47uf_0805 to 22uf_0603 meet ME height limitation.
Page 17-- R474 change value from 0 ohm to 36K ohm, mount AC41 0.1uf to meet AU1 turn on timming.
Page 18-- R522,R523,R524,R525 change value from 150ohm to 140ohm, for EMI.
Page 19-- Add R5294,R5295 by NEC.
Page 19-- non-staff Q52,Q56, and C520,C521 change the value from 2200pf cap to 0ohm resistor ,DPTF has not use the Q52,Q56.
Page 7-- Reserved R5296、R5297、R5298 by NEC
Page 20-- C96,C102,C456,C457 change size to 0805
Page 19-- Add R5293 for ESD.
Page 2,4,8,10,14~18,20,21-- Short 0ohm Location:R113;R286,R287,R265,R325,R232,R228;R421;
R492,R394,R379,R402,R396,R273,R399,R412,R391,R409,R407,R403,R271,R408,R272,R274,R411,R405,
,R410;R349,R348,R343;R338,R334,R460,R462,R461;R6,R7,R8,R9,R12,R5266,R5267;R5265,AR22;R5239;R197;R72
Page 4,9,17,22-- Short 0ohm Location:R753,R755,R756,R757;R175,R176,R177,R178,R94,R102;AR21;R5252
Page 7-- C119,C120 change value from 15pf to 12pf to follow vendor's suggestion.
Page 23--
change PR26 from 1.02k ohm to 1.27k ohm to correct OC.LL and IMON.
change PC29 from 470pF to 220pF to correct DVID response.
change PR37 from 97.6k to 115k ohm to correct IMON.
change PR33 from 102k to 93.1k to correct IMON
change PR68 from 2.26k ohm to 2.67k ohm to correct LL
Page 10-- Staff C8715、C8716、C8717、C8718 for power noise.
Page 10-- mount C456,C96 47uf,and C457,C102 change value from 22uf to 47uf to support NEC ODD.(3A)

Change history (ES2 to PP)

Change history (PP to MRT)